PAA5102E1-M: Optical Tracking Miniature Chip

General Description

The PAA5102E1-M is a high performance and highly accurate optical tracking chip using PixArt LASER/LED hybrid optical navigation technology. It integrates an optical chip with a LASER light source in a single miniature package. When working with an external infrared LED and a PixArt designed companion lens LST0-217, the chip can track on a wide range of material surfaces from white glossy tiles to shag carpets. Besides, the sensor also provides a high DOF range to accommodate uneven surfaces when tracking.

Key Features

- Reflowable SMT package with built-in VCSEL LASER light source in a single package
- LASER/LED hybrid optical navigation technology
- Compliance to IEC/EN 60825-1:2014 Eye Safety with Class 1 LASER power output level
- Tracking on glossy surfaces (metal, tiles) via LASER and diffused surface (cloth, carpets) via LED
- Wide working range from 40mm – 60mm
- High tracking accuracy
- Support 3-wire SPI interface
- Programmable resolution

Applications

- Devices that require tracking on surfaces with wide working range
- Devices that require tracking on a surfaces with wide range of material surfaces
- Devices that require speed detection and distance of moving surfaces

Key Parameters

Parameter	Value
Supply Voltage	VDD : 2.7 to 3.6V
Control Interface	3-wire SPI
Companion lens	LST0-217
Light Source	Infrared 850nm LED Infrared 850nm LASER
Tracking Speed	Up to 15 ips (LASER mode) Up to 30 ips (LED mode)
Power Consumption (@ VDD = 3.3V)	Run mode : 11.5mA (LASER mode) 44mA (LED mode) Power down : 15µA
Working Range (Distance from PCB surface to reference plane)	40 to 60mm (Reference plane: the top of the surface)
Package Size L x W x H	4.6 x 4.4 x 1.0 mm^3

Ordering Information

Part Number	Package Type
PAA5102E1-M	10-pin LGA Package
LST0-217	Lens Set

RoHS compliant

LASER 1

For any additional inquiries, please contact us at https://www.pixart.com

Table of Contents

List of Figures

List of Tables

1.0 Introduction

1.1 Overview

PAA5102E1-M is a high performance CMOS-process optical image chip with integrated digital image process circuit. It is based on PixArt LASER/LED hybrid optical navigation technology which measures changes in position by optically acquiring sequential surface images (frames) and mathematically determining the speed, direction and the magnitude of motion. The displacement X and Y information are made available in registers. A host controller can read and translate the displacement X and Y information via SPI serial interface.

Since LASER and LED are not allowed to be turned on at the same time, the host controller should keep reading the Image Quality registers to determine if LASER or LED should be chosen to illuminate the surface. In general, when LASER is chosen for illumination, the Image Quality value is high when tracking on tiles and low when tracking on carpets. On the contrary, when LED is chosen for illumination, the Image Quality is high when tracking on carpets and is low when tracking on tiles.

Note: Throughout this document PAA5102E1-M is referred to as the chip.

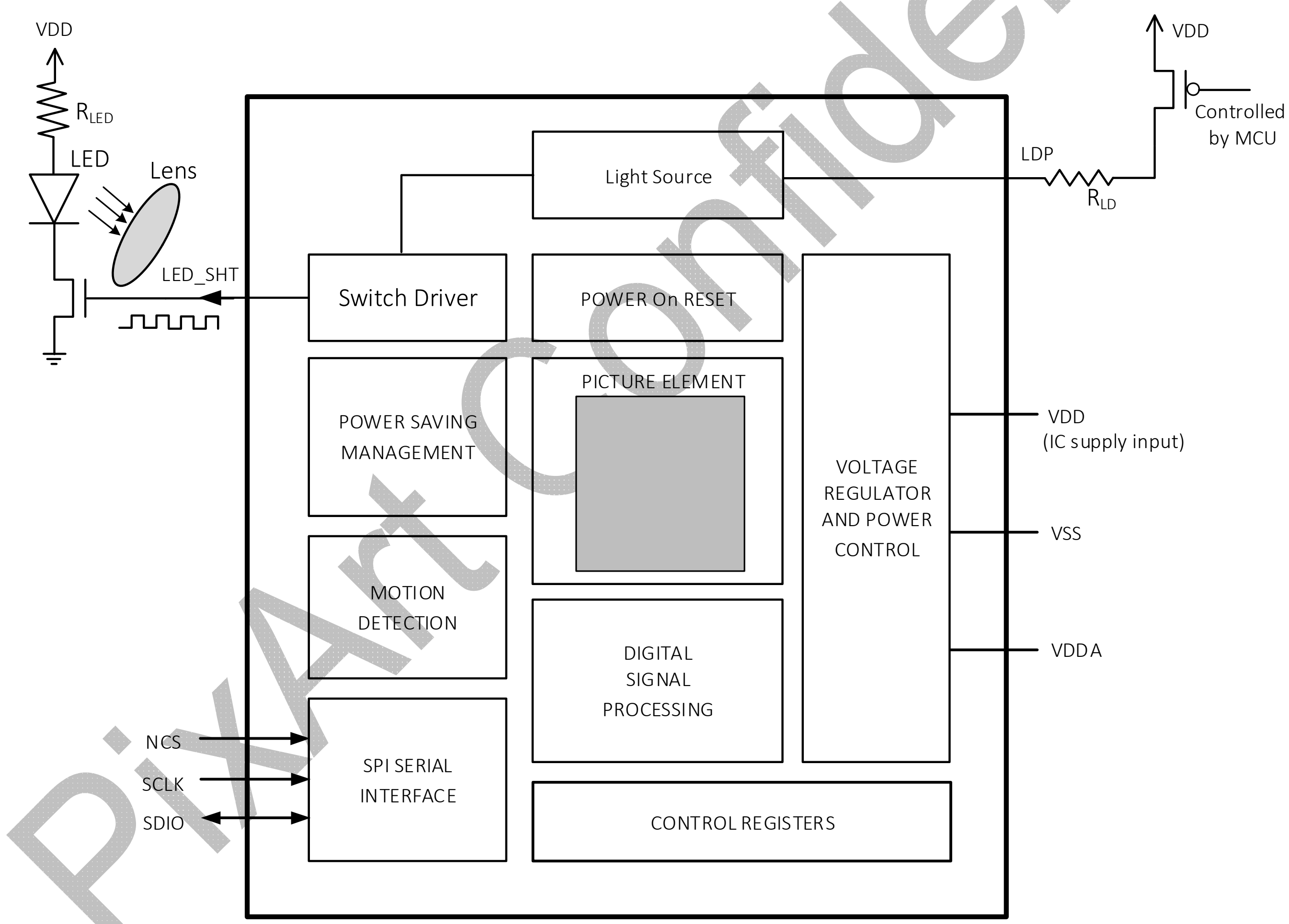
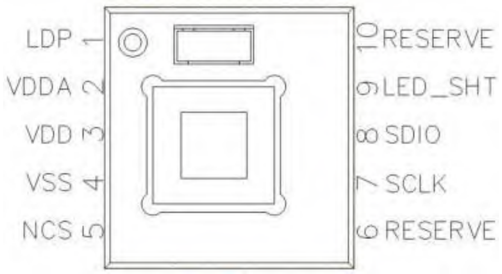


Figure 1. Chip Architecture Functional Block Diagram

1.2 Signal Description



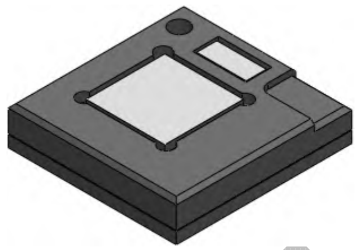


Figure 2. Pinout Configuration

Table 1. Signal Pins Description

Pin No.	Signal Name	Type	Description
1	LDP	Power	Anode of the VCSEL LASER. This pin should be connected to VDD (2.7 to 3.6V) through a resistor (RLD).
2	VDDA	Power	Internal 1.8V regulator output
3	VDD	Power	Power supply for I/O and LASER, voltage range : 2.7 to 3.6V
4	VSS	Ground	Chip ground
5	NCS	Input	Chip select for 3-wire SPI interface (active low)
6	RESERVE	NC	This pin should connect a 100k ohm resistor to Ground.
7	SCLK	Input	Clock input for SPI interface
8	SDIO	I/O	Bi-directional I/O for SPI interface
9	LED_SHT	Output	LED Shutter. The shutter control for the external LED light source
10	RESERVE	NC	This pin should connect a 100k ohm resistor to Ground.
1	LDP	Power	Anode of the VCSEL LASER. This pin should be connected to VDD (2.7 to 3.6V) through a resistor (RLD).
2	VDDA	Power	Internal 1.8V regulator output

2.0 Operating Specifications

2.1 Absolute Maximum Ratings

Table 2. Absolute Maximum Ratings

Parameters	Symbol	Min.	Max.	Unit	Notes
Supply Voltage	VDD	-0.3	3.9	V	I/O and LASER power
	VDDA	-0.2	2.3	V	Core circuitry power
ESD	ESD_{HBM}		2	kV	Class 2 on all pins, as per human body model. JESD22-A114E with 15 sec zap interval.

Notes:

1. At room temperature.
2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum-rated conditions is not implied.

2.2 Recommended Operating Conditions

Table 3. Recommended Operating Conditions

Description	Symbol	Min.	Typ.	Max.	Unit	Notes
Storage Temperature	T_{STG}	-40	-	85	°C	
Operating Temperature	T_A	-20	25	60	°C	
Power Supply Voltage	VDD	2.7	3.3	3.6	V	I/O and LASER power supply
Supply Noise (peak to peak)	V_{pp}	-	-	100	mV	Peak to peak voltage within 100KHz – 80MHz
SPI Clock Frequency	SCLK	-	-	2	MHz	
Tracking Speed	SP	-	-	15	IPS	on white tile (LASER mode)
				30		on specific wooden flooring (LED mode)
Laser Drive Current (DC)	I_{LD}	5.0	7.0	8.0	mA	Configure via LD_SRC register
Working Range (Distance from PCB surface to reference plane)	Z	40	50	60	mm	Reference plane: the top of the tracking surface. Please refer to the figure below.

Note: PixArt does not guarantee the performance if the operating temperature is beyond the specified limit.

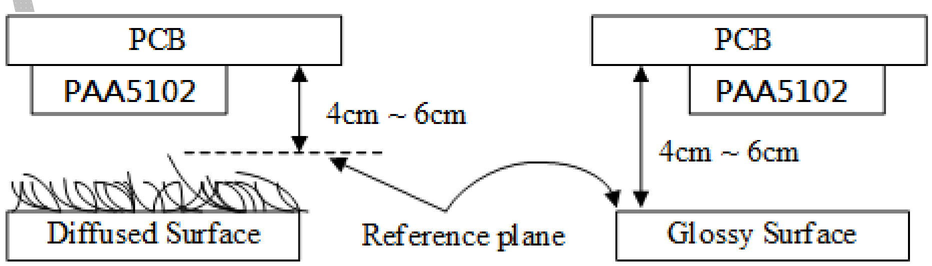


Figure 3. Distance from bottom of PCB to reference plane

2.3 DC Characteristics

Table 4. DC Electrical Specifications

Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
Power Consumption	I_{VDDRN}	-	 10 11.5 11	-	mA	LASER Run mode for White Tile for Black Tile for Wooden Flooring
			44		mA	LED Run mode
	I_{VDDPD}		15		µA	VDD current @power down
I/O Input High Voltage	V_{IH}	0.7 x V_{DD}	-	-	V	
I/O Input Low Voltage	V_{IL}	-	-	0.3 x V_{DD}	V	
I/O Output High Voltage	V_{OH}	V_{DD} - 0.4	-	-	V	@I_{OH} = 2mA
I/O Output Low Voltage	V_{OL}	-	-	0.4	V	@I_{OL} = 2mA

Notes: All the parameters are tested under operating conditions: V_{DD} = 3.3V (including LASER current), T_A = 25°C

3.0 Mechanical Specifications

3.1 Package Mechanical Dimension

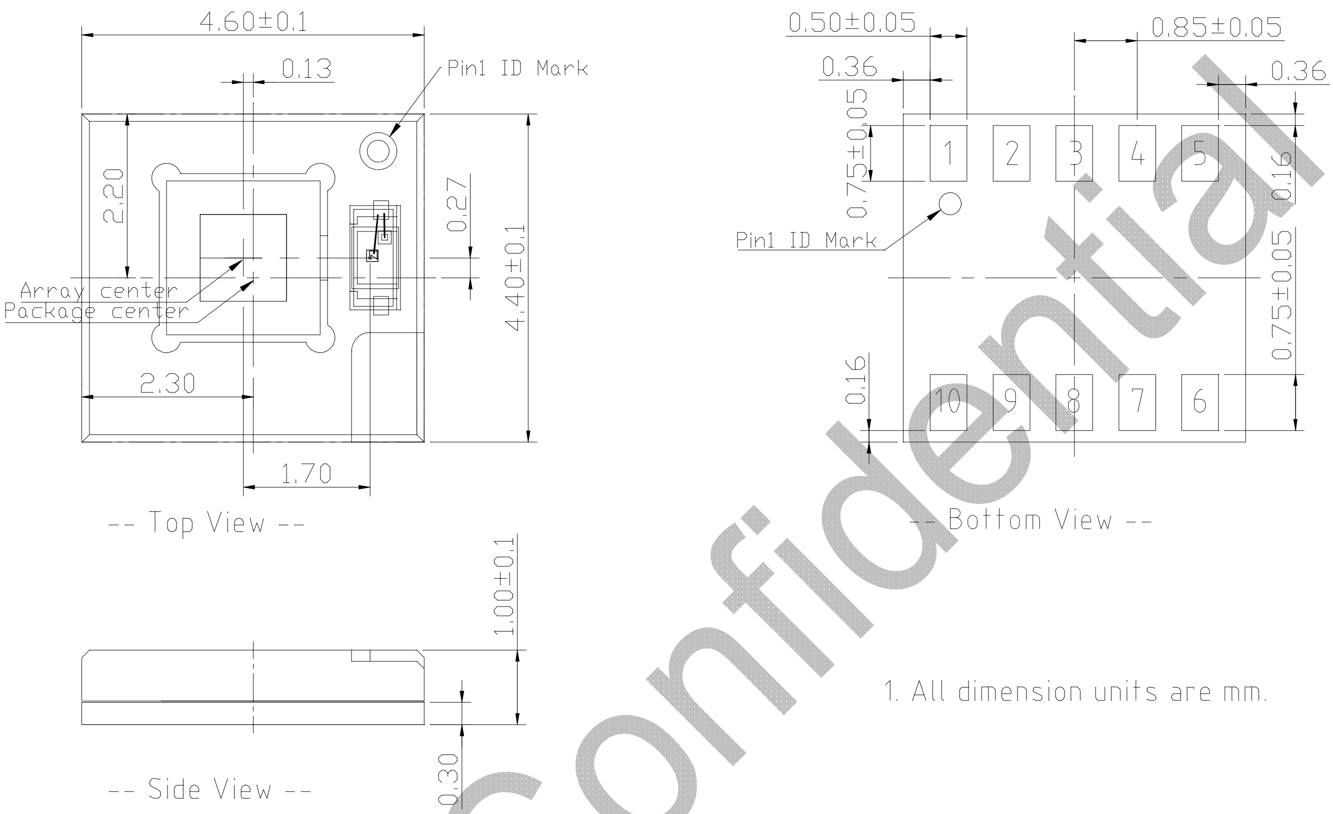


Figure 4. Chip Package Outline Diagram

3.2 Lens Mechanical Dimension

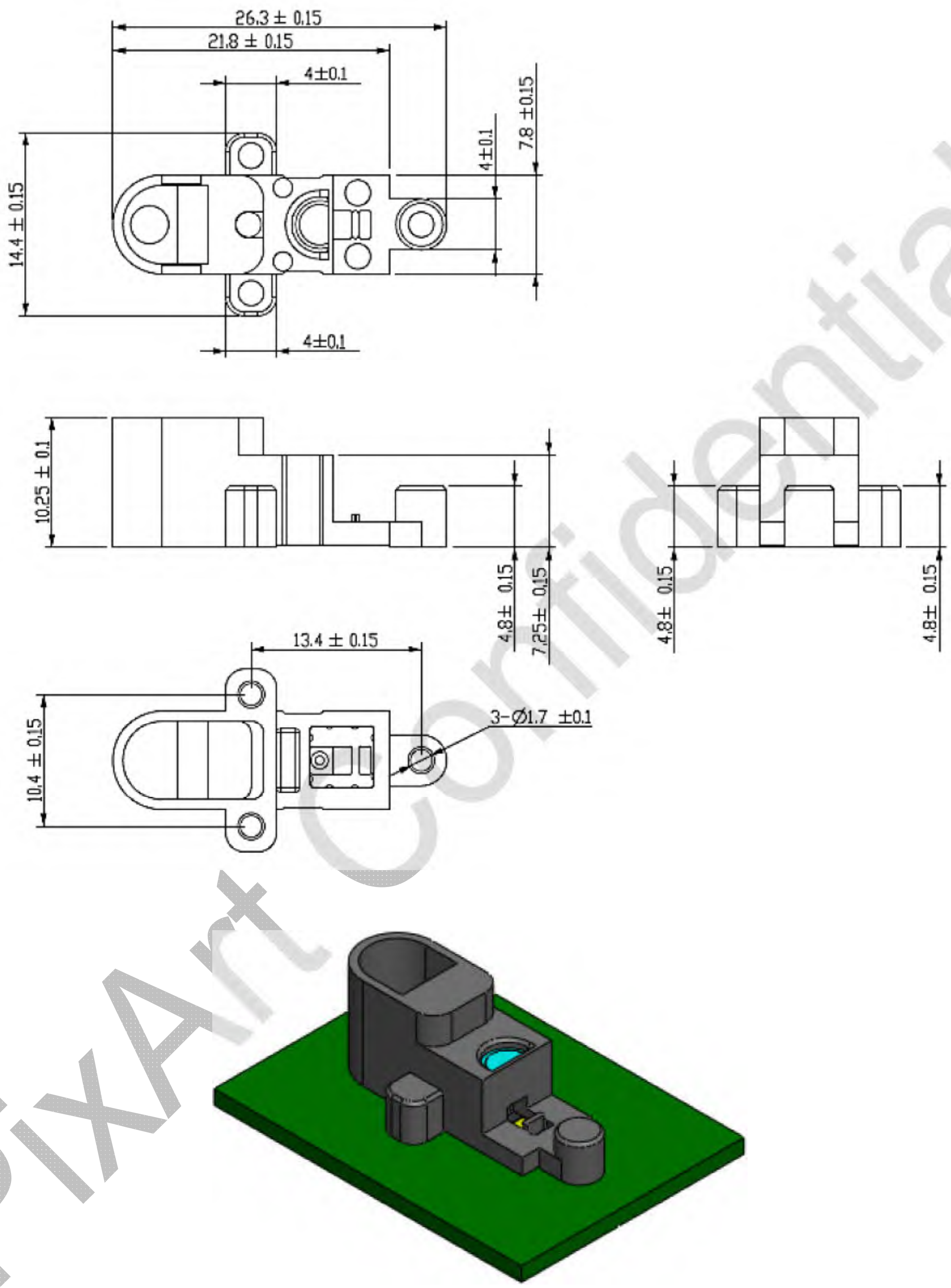


Figure 5. Lens Mechanical Dimensions

3.3 PCB Layout Guides

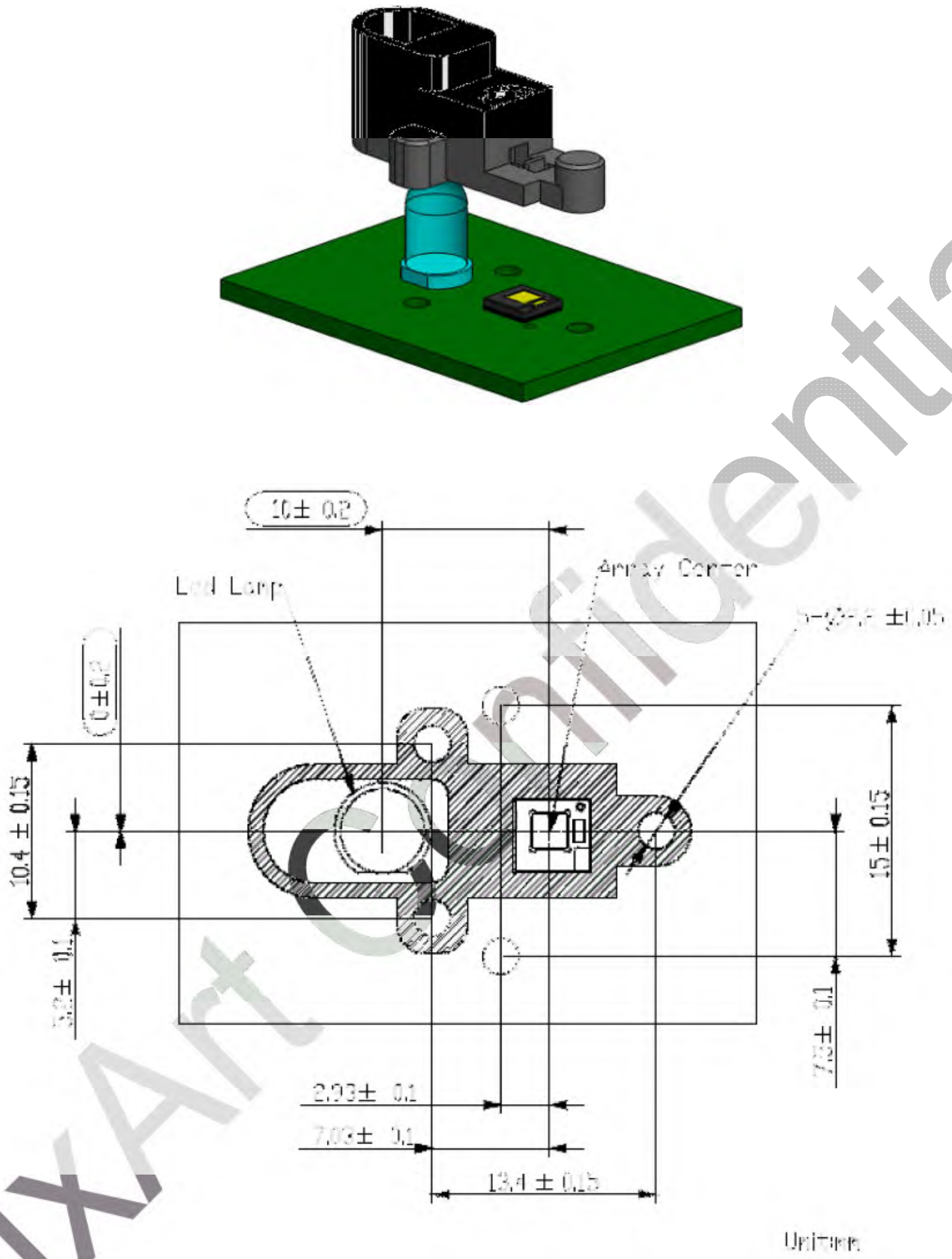
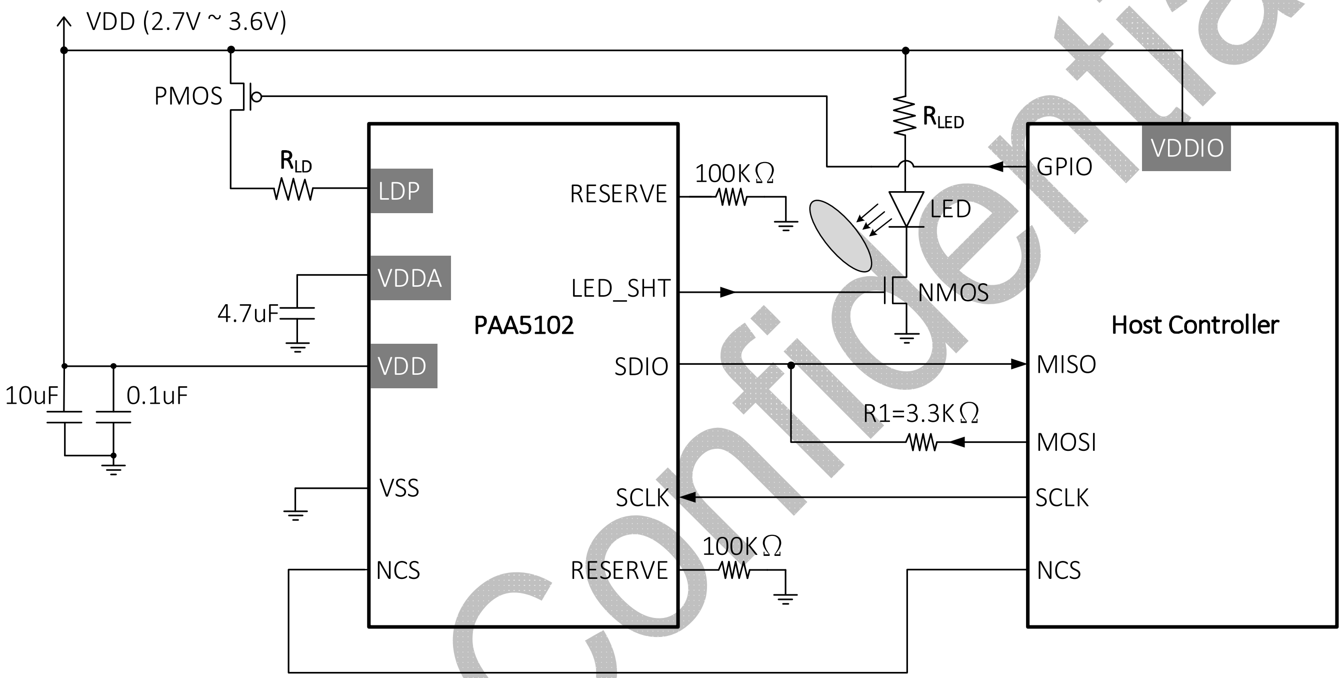


Figure 6. PCB Layout Guides

4.0 Design Reference

4.1 Reference Application Schematics

The chip only supports simplified 3-wire SPI slave mode, while some host controllers may only support standard 4-wire SPI master mode. In this case, users can connect the host controller to the chip using the method shown below to communicate with each other. Take note that the 3.3K ohm resistor (R1) is for reference only and the resistance may have to be modified according to different I/O capability as per the specification of the host controllers. The resistor R_{LD} and R_{LED} are to restrict the current flowing through the LASER and LED. In order not to overdrive the LASER and LED, please adopt the resistance specified in the table.



VDD (Volt)	R_{LD}(ohm) +/-3%	R_{LED}(ohm) +/-3%
3.6	177	19
3.5	165	18
3.4	152	17
3.3	140	15
3.2	128	14
3.1	115	13
3.0	102	12
2.9	90	11
2.8	78	10
2.7	65	9

Figure 7. Reference Application Schematics

4.2 Power-up Sequence Requirements

To avoid occurrence of unexpected chip instability, a power-up sequence needs to be applied upon power up.

1. POR (power on reset) circuit is embedded in the chip with a POR voltage of 1.8V, so no external power on reset circuit is needed. A timing ($t_{ZERO-POR}$) is required to ensure the chip is initialized properly.
2. SPI control is valid at least 10ms (t_{ON-SPI}) after a stable VDD power supply is applied to the chip.

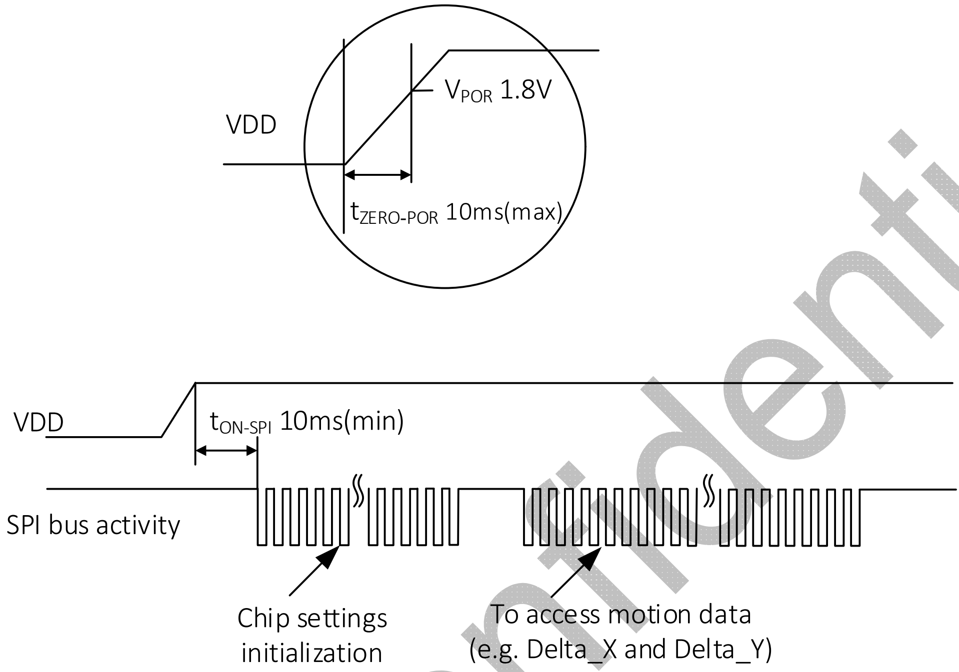


Figure 8. Power-up Sequence Requirements

Table 5. Power-up Sequence Specifications

Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
Power ON Reset Voltage	V_{POR}	-	1.8	-	V	
Power Applied from Zero to POR Time	$t_{ZERO-POR}$	-	-	10	ms	
Power Stable to SPI Valid Time	t_{ON-SPI}	10	-	-	ms	

Notes: All the parameters are tested under operating conditions: V_{DD} = 3.3V, T_A = 25°C

5.0 3-Wire SPI Serial Interface

The chip supports 3-wire Serial Peripheral Interface (SPI). The host controller can use the SPI to write and read registers in the chip, and to read out the motion information. The host controller always initiates communication; the chip never initiates data transfers. NCS, SCLK and SDIO may be driven directly by the host controller. SDIO may also be driven by the chip when data is read out from chip registers.

- NCS: Chip select input (active low). NCS needs to be low to activate the SPI; otherwise, SDIO will be at high-Z state and SCLK will be ignored. NCS can also be used to reset the SPI in case a communicational error happens.
- SCLK: Clock input. It is always generated by the host controller.
- SDIO: Bi-directional input/output data

5.1 Transmission Protocol

The transmission protocol is a 3-wire link, half duplex protocol between the host controller and the chip. All data changes on SDIO are initiated by the falling edge on SCLK. The host controller always initiates communication; the chip never initiates data transfers. The transmission protocol consists of the following two operation modes.

- Write Operation
- Read Operation

Both of the two operation modes consist of two bytes. The first byte contains the address (seven bits) and has a bit-7 as its MSB to indicate data direction. The second byte contains the data.

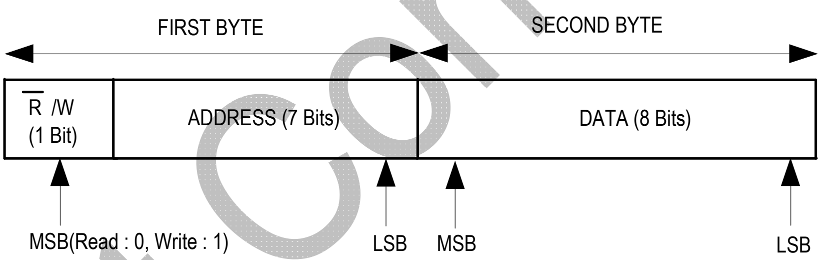


Figure 9. Transmission Protocol

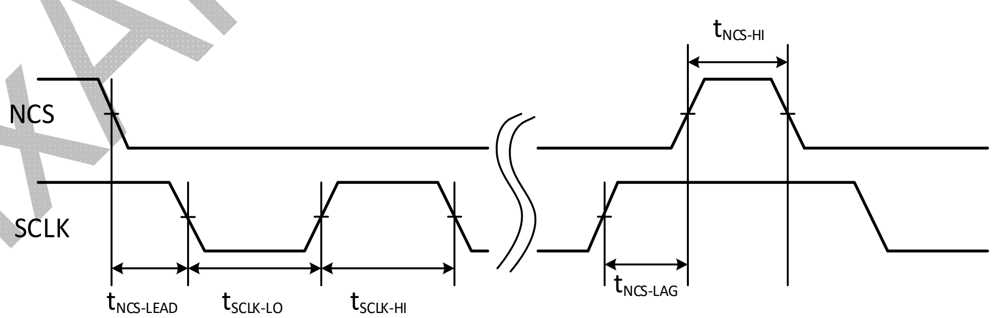


Figure 10. NCS vs SCLK Timing Requirement

5.1.1 Write Operation

A write operation, defined as data going from the host controller to the chip, is always initiated by the host controller and consists of two bytes. The first byte contains the address (seven bits) and has a "1" as its MSB to indicate data direction. The second byte contains the data. The communication is synchronized by SCLK. The host controller changes SDIO on the falling edges of SCLK and the chip reads SDIO on the rising edges of SCLK.

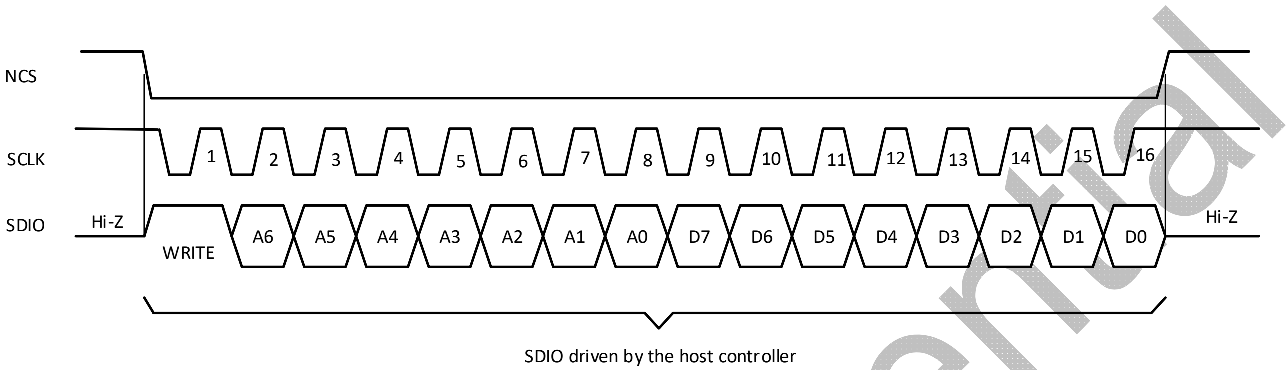


Figure 11. Write Operation

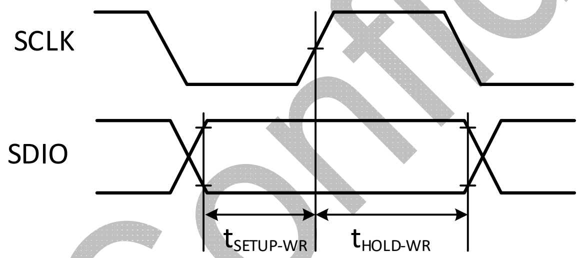


Figure 12. SDIO setup and hold time during write operation

5.1.2 Read Operation

A read operation is initiated by the host controller and consists of two bytes. The first byte contains the address specified by the host controller and has a "0" as its MSB to indicate data direction. The second byte contains the data which is output by the chip. The communication is synchronized by SCLK. SDIO is changed on the falling edges of SCLK and is read on every rising edge of SCLK. The host controller must release SDIO bus and handover the control of SDIO bus to the chip on the falling edge of the last address bit.

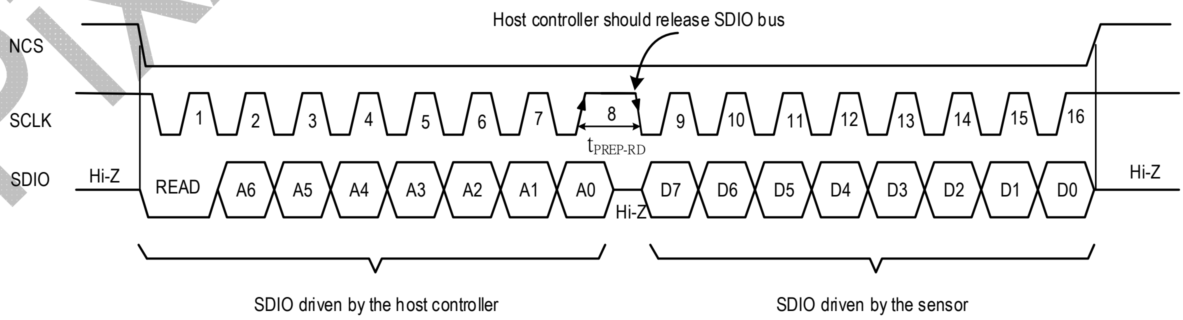


Figure 13. Read Operation

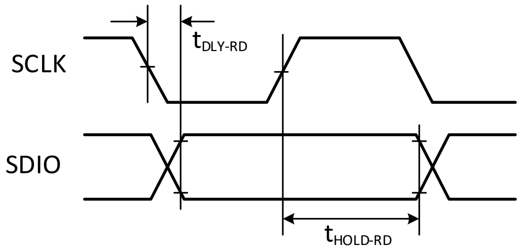


Figure 14. SDIO delay and hold time during read operation

5.2 SPI Timing

Table 6. SPI Timing Specifications

Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
SCLK frequency	f_{SCLK}	-	-	2	MHz	SPI max. operation frequency
SCLK High Time	$t_{SCLK-HI}$	250	-	-	ns	SCLK min. high time
SCLK Low Time	$t_{SCLK-LO}$	250	-	-	ns	SCLK min. low time
NCS Enable Lead Time	$t_{NCS-LEAD}$	1	-	-	µs	From NCS falling to first SCLK falling
NCS Enable Lag Time	$t_{NCS-LAG}$	1	-	-	µs	From Last SCLK rising to NCS rising
NCS min. High Time	t_{NCS-HI}	2	-	-	µs	From previous NCS rising to next NCS falling
SDIO Write Setup Time	$t_{SETUP-WR}$	250	-	-	ns	SDIO data valid before SCLK rising
SDIO Write Hold Time	$t_{HOLD-WR}$	250	-	-	ns	SDIO data valid after SCLK rising
SDIO delay after SCLK	t_{DLY-RD}	-	-	100	ns	From SCLK falling to SDIO data valid, no load conditions
SCLK delay for Data Preparation	$T_{PREP-RD}$	250	-	-	ns	From rising SCLK for last bit of the address byte, to falling SCLK for first bit of data being read
SDIO Read Hold Time	$t_{HOLD-RD}$	250	-	-	ns	SDIO data valid after SCLK rising
SDIO Rise Time	t_{SDIO-R}	-	30	-	ns	@C_L = 30 pF
SDIO Fall Time	t_{SDIO-F}	-	30	-	ns	@C_L = 30 pF

6.0 Read Motion Data

Whenever the chip detects the occurrence of motion, the detected motion data (X-movement and Y-movement) is accumulated and stored in chip's internal buffer. The host controller can read out this motion data through register Delta_X (address 0x03 and 0x011) and Delta_Y(address 0x04 and 0x12). Before reading the motion data through these registers, be sure to read register Motion_Status (address 0x02) first to check if the MOTION bit (bit 7) is 1. If the MOTION bit is 1, the data in register Delta_X and Delta_Y are valid, otherwise it is invalid. By reading and checking register MOTION Status (address 0x02) periodically, the host controller can get the motion data in a simple way through the SPI interface. Note that the 8ms shown in the flowchart below is just a reference. The delay time might depend on the capability of the host controller and the need for different applications.

Also, in order to track on a wide range of surface material, the light source for illumination has to be switched between LASER and LED. The host controller should monitor the IQ value of the surface and if the IQ value is too low (lower than a predefined value, IQ_THD, which is stored in the host controller), the host controller has to switch the existing light source and change other related register settings as well.

Note: the flowchart below just shows one of the methods to switch between LED mode and LASER mode. Different applications might need different methods to implement this switch function.

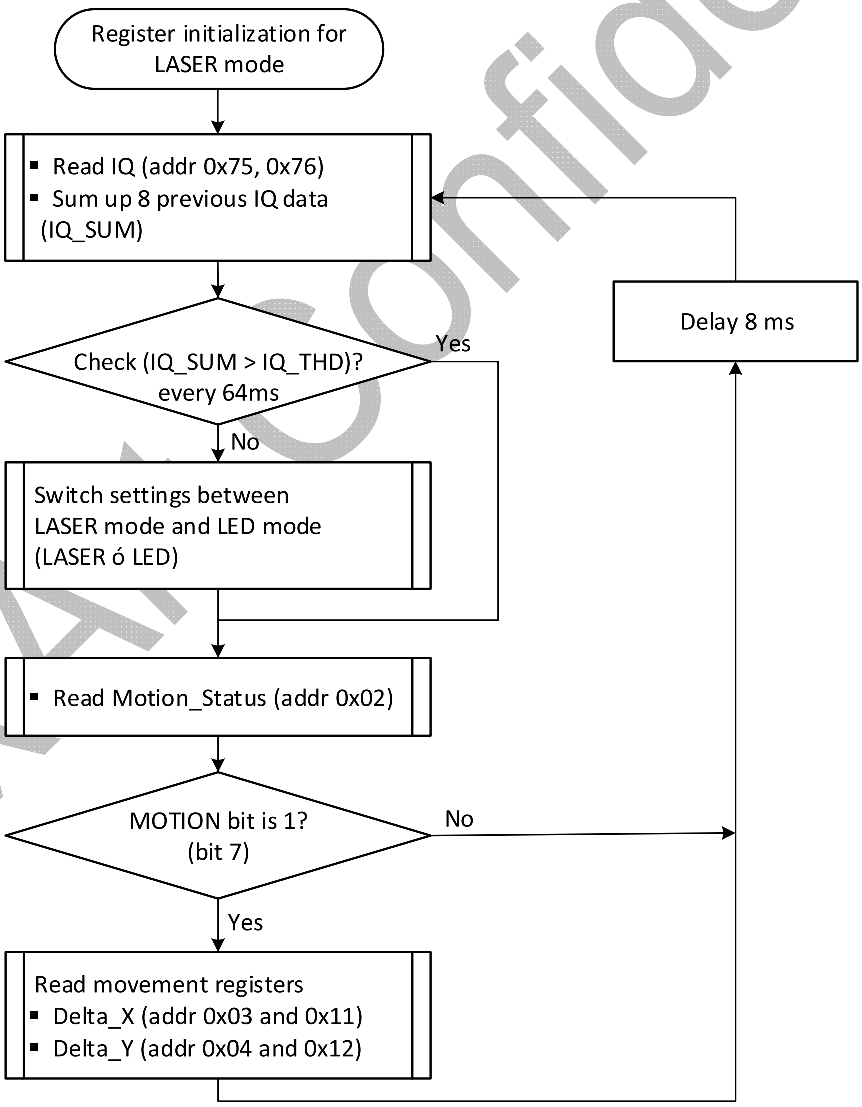


Figure 15. Read Motion Data with Polling Mode

7.0 Software Control Functions

7.1 Software Power-Down

The chip can also be put into the lowest power state (power-down mode) by setting PD_EnH bit (bit 3) in the Configuration register (address 0x06) through SPI interface. In power-down mode, all the chip register settings are retained and can be accessed through SPI interface as well. Reset PD_EnH bit will get the chip out of the power-down mode. To obtain correct motion data, it is recommended that the host controller should wait at least 3ms before reading the motion data after resetting the PD_EnH bit.

7.2 Software Reset

During power-up, the chip does not need an external power-on reset as there is an internal circuitry that performs power-on reset function in the chip. However the chip can also be reset by setting the RESET bit (bit 7) of Configuration register (address 0x06). Upon a software reset being executed, all the register values will be reset to the power-up default values and all the recommended register settings must be reloaded for proper operation of the chip.

8.0 LASER Drive

8.1 LASER Drive Control

Under normal operating condition, the chip internally generates the drive current for the integrated LASER diode in pulsing mode. The LASER drive current source is configurable via LD_SRC register (address 0x51) with power-up default setting of LD_SRC[4:0] = 0x0E which is equivalent to ~17mA in continuous mode; while the maximum drive current could be up to ~37mA when LD_SRC[4:0] = 0x1F. However, the software setting **MUST** limit any value beyond LD_SRC[3:0] = 0x06 that drive >8mA current. The recommended setting for common surface tracking application is LD_SRC[4:0] = 0x06 (~7.2mA drive current).

An external current limiting resistor, R_{LD} connecting the VDD to LDP pin via a switching PMOS is mandatory to be included in any design application circuit of final product to limit the overcurrent condition during the system power-up. The VDD power supplies for the chip should be well regulated and filtered to prevent spurious voltage conditions at all time. The recommended circuit connection of R_{LD} is shown in Section 4.1 Reference Schematics.

Caution: The overdriving of LASER beyond the specified LASER drive current in Table 3. Recommended Operating Conditions could cause the following consequences.

1. The LASER output may exceed the Laser eye safety limit resulting in hazardous radiation exposure.
2. The LASER output may degrade in the long run or could be damaged (the worst case scenario).

8.2 LASER Output Power

The LASER eye safety limit of the sensor is at the LASER output power of 716µW with the LASER drive current not exceeding 8mA in continuous mode. Since the LASER drive is always pulsing during sensor operational mode, the average LASER power will never exceed the LASER eye safety limit. As the LASER drive control pin to the LASER's Cathode pin is bonded internally in the chip package, the risk to externally drive the LASER in continuous mode is relatively low. Thus, the system design of PAA5102E1-M is claimed to be compliant to LASER Eye Safety Class 1 (IEC/EN 60825-1:2014).

8.3 Precautions

The manufacturer of the end product is responsible to ensure that the end system design is taking the following steps into considerations.

1. The software setting of the LASER drive control register does not exceed the maximum allowable LASER drive current specification as listed in Table 3. Recommended Operating Conditions.
2. The external current limiting resistor, RLD, should be well connected between LDP pin and VDD. Please refer Section 4.1.
3. Do not use any controls or adjustments of procedures other than those specified in this document that may cause the Laser output power beyond the eye safety limit.
4. Laser eye safety responsibility resides at the system level, not at the component level, thus the manufacturer of the Laser Product should provide the user instruction or a user manual that contains all Laser eye safety information.
5. The final product should have a visible label to alert the end user on the potential danger of LASER to the unprotected eyes.
6. Any users of this sensor and its system in an unfinished product must be aware and need to take the precautionary steps to avoid being exposed to the LASER at all times.
7. All users who will be working with an active (powered) sensor component should consider taking LASER eye safety training.
8. The LASER light is in the infrared spectrum of 850 nm. It is not intended to be viewed so users should not try to look at the sensor's aperture directly. Appropriate instrument for indirect viewing is recommended.
9. It is a must to follow the LASER Drive Control during the operation of this sensor and its system.