DB2015V

HomePlug Green PHY Module

Specification 1.0.18

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[DB-xxxxxxx] ([Development Status][x]), ref [DB-yyyyyyy] ([Development Status][y])

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1 OVERVIEW

DB2015V Module, based on HomePlug Green PHY technology, delivers a set of hardware module, software and service solution for Supply Equipment Communication Controller (SECC), and Electric Vehicle Communication Controller (EVCC).

1.1 HomePlug Green PHY

The module supports fully HomePlug Green PHY Spec 1.1(IEEE 1901). HPGP Features:

- Spectrum: 2-30MHz
- Max PHY Rate: 10Mbps
- Modulation: OFDM
- Subcarriers: 917
- Subcarrier Space: 24.414KHz
- ROBO: 4Mpbs (5x Repeat Code) 5Mbps (4x Repeat Code) 10Mpbs (2x Repeat Code)

1.2 Compatibility

The module is compliant to below protocols:

- ISO 15118-3
- DIN 70121
- SAE J2931/4
- GB/T 27930 Functionality with External MCU.

1.3 Module Diagram

The block diagram in Figure 1 shows the module components in the gray box as well as the connections and external components that needed in addition.

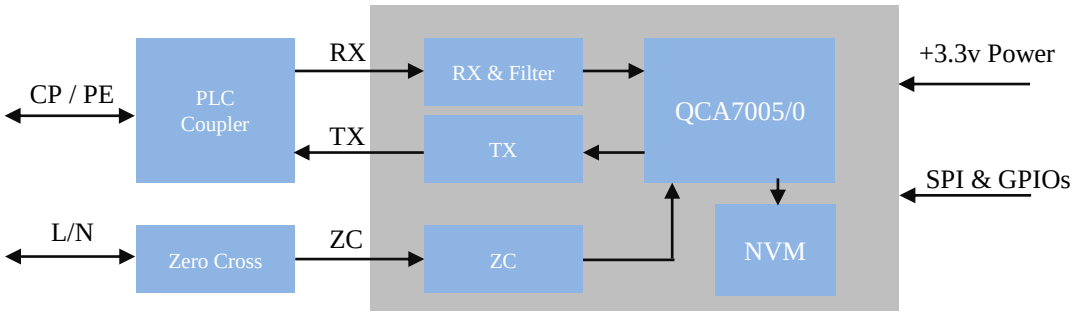


Figure 1: Block Diagram of DB2015V

All parts are located below a metal shield. Information about the module is printed on a high-temperature label on top of this shield.

1.4 Host Interface

DB2015V module provides SPI Slave interface which uses the standard 4-wire Motorola-SPI protocol plus an interrupt pin to Host CPU.

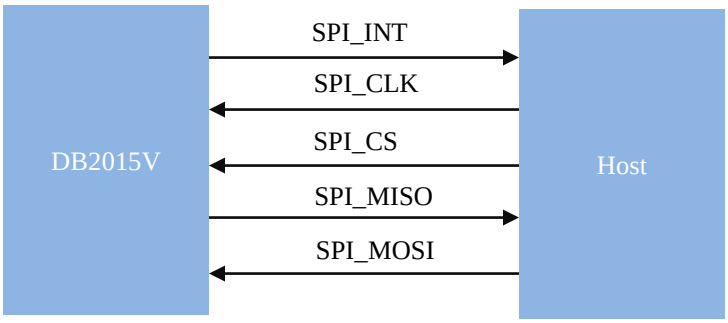


Figure 2: Block Diagram of SPI Slave Signal Pins

Notes:

(1) The DB2015V SPI bus role is **SLAVE**.

(2) Support 16Mbps baud rate (Max).

Signal	Description
SPI_CLK	SPI slave input clock signal driven by the host during a bus transaction.
SPI_CS	Bus qualifier to select the QCA7005/0 device in case the device is in a shared bus-arrangement with other peripherals. The SPI slave tri-states SPI_MISO, when CS is de-asserted as well as ignore any data issued on SPI_MISO (Will not interpret SPI frames).
SPI_MOSI	The master-out-slave-in signal. This is driven by the master to indicate a bus command or data (write data).
SPI_MISO	The master-in-slave-out signal. This is return path of read data requested by the master.
SPI_INT	QCA7005/0 pending interrupt signal, active high.

The SPI host bus controller should support the following features:

- Minimum of 8-bit data framing (16-bit is recommended)
- Clock Phase and Polarity control (Requires SPI-Mode-3 clock Phase and Polarity)
- Level triggered interrupt for DB2015V_SPI_INT line. This signal must be mask-able by software.

For optimal performance, the following features should be considered:

- 16 and 32-bit data framing (reduces inter-frame gaps for CS assertion)
- SPI-controller DMA support for large SPI data frame sequences

2 MODULE INFORMATION

2.1 General

Figure 3: Image of DB2015V

2.2 Pin Definitions

Pin	Name	Usage
1	GND	Module Ground
2	RX-	Power Line Coupling Transformer Rx-
3	RX+	Power Line Coupling Transformer Rx+
4	GND	Module Ground
5	TX-	Power Line Coupling Transformer Tx-
6	TX+	Power Line Cooping Transformer Tx+
7	GND	Module Ground
8	GND	Module Ground
9	ZC_IN	Power Line Zero Cross in. Note: if not use, connect it to Ground
10	GND	Module Ground
13	GPIO[0]	Boot Source Selection: High, NVM; Low, Host.
14	GPIO[1]	Don't use.
15	GPIO[2]	SPI Mode Selection: High, Burst; Low, Legacy.
16	GPIO[3]	Output for LED. SECC: It will be ON when the device acts as CCo with authenticated STAs. EVCC: It will be ON when the device is associated as well as authenticated to AVLN.
17	/Reset	Module Reset. Low active; Pulled up by 10k Resistor in module

18	SPI_MOSI	Serial In for SPI interface
19	SPI_MISO	Serial Out for SPI interface
20	SPI_CS	Serial CS for SPI interface
21	SPI_CLK	Serial CLK for SPI interface
22	SPI_INT	Serial Interrupt for SPI interface
23	GND	Module Ground
24	+3.3v	Power Supply. 3.3v
25	GND	Module Ground

2.3 Power on Configuration

The QCA7000 / QCA7005 comprise four GPIO pins which are read at boot time to get the desired configuration.

GPIO	Function	Pull Up	Pull Down	Preload on Module
[0]	Boot Source	NVM	Host	10k Ohm Pull Up
[1]	Host Interface	-	SPI Slave	10k Ohm Pull Down
[2]	SPI Slave Mode	Burst	Legacy	10k Ohm Pull Up
[3]	None	-	-	-

2.4 Form Factor

Width*Length*Height: 25*34.06*4mm

2.5 Recommended Footprint

Recommended Footprint:

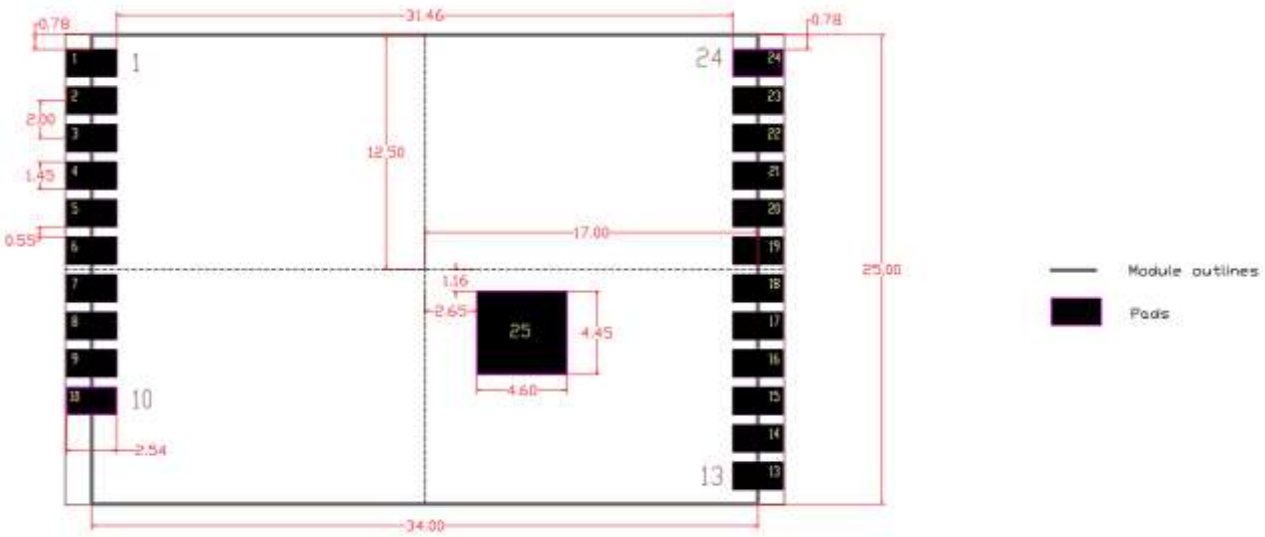


Figure 5: Recommended Footprint

Notes:
1. All dimensions are in mm; the height is about 4mm.
2. Pads are all of the same size.
3. Distances between pads are equal if not otherwise specified in the drawing.
4. The drawing shows the top view on the footprint (as if you look through the module).
5. The module outline shows the ideal measures - tolerance is not included.

3 ELECTRICAL CHARACTERISTICS

3.1 Recommended Operating Rating

Symbol	Parameter	Min	Typ	Max	Units
+3.3V	Power Supply	3.13	3.3	3.46	V

3.2 Environment Storage Condition

Environment condition	
Temperature	Operating Temperature: -40 deg.C ~85 deg.C
	Storage Temperature: -40 deg.C ~105 deg.C

3.3 DC Switching Thresholds

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{IL}	Low-level input voltage		—	0.8	V
V_{IH}	High-level input voltage		2.0	—	V
Symbol	Parameter	Test Conditions	Min	Max	Units
VOL	Low-level output voltage	IOL= 4 mA, 12 mA[1]	—	0.4	V
VOH	High-level output voltage	IOH = -4 mA, -12 mA[2]	2.4	—	V
IIL	Low-level input current	VI = Gnd	-1	—	µA
IIH	High-level input current	VI = Vdd	—	1	µA
IOZ	High-impedance output current	Gnd≤VI≥Vdd	-1	+1	µA

1. IOL = 12 mA for all GPIOs
   IOL = 4 mA for all other interfaces
2. IOH = -12 mA for all GPIOs.
   IOH = -4 mA for all other interfaces

3.4 Power Dissipation

Parameter	Value
Max Power Dissipation	250mA
Typical Power Dissipation	200mA

4 EV CHARGING APPLICAION

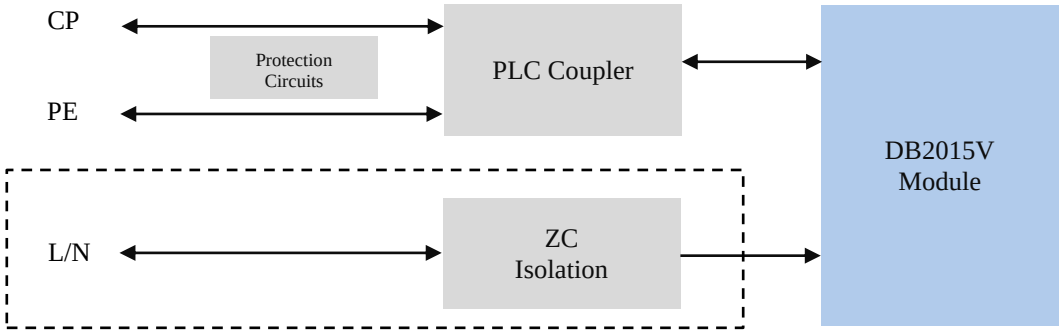


Figure 5: DB2015 EV Charging Application

Note: The EVCC application, Zero Cross circuits are not needed.

4.1 DB2015V Reference Application

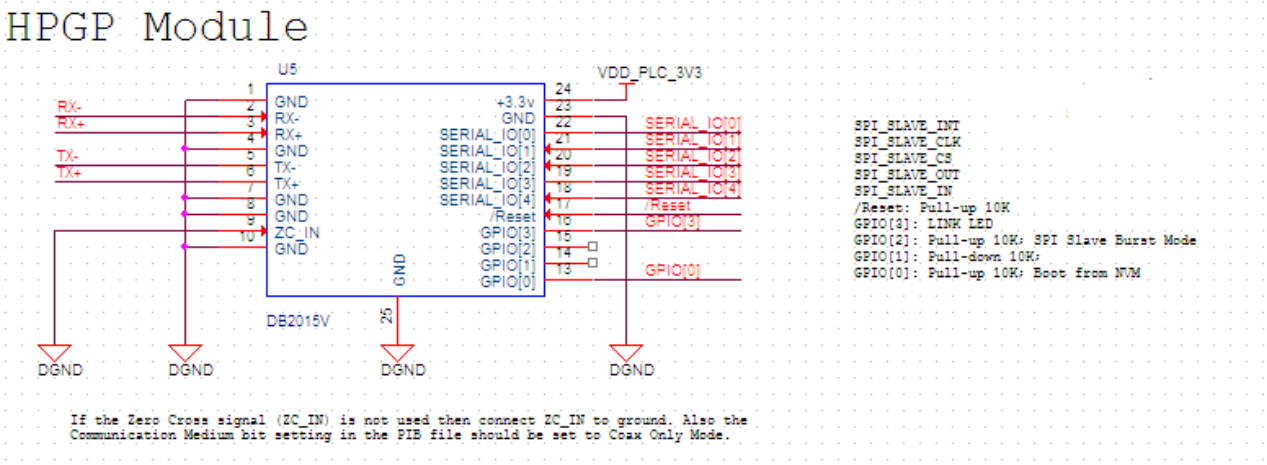


Figure 6: DB2015V Reference Application

The pre-configuration of DB2015V is below:

Configuration	Status	Description
GPIO[0]	Pull-up	Module runs with the preprogrammed firmware.
GPIO[1]	Floating	Floating in all applications.
GPIO[2]	Pull-up	SPI Slave bus uses burst mode.(1)

ZC_IN	Pull-down	Pull-down in all EVCC applications.
Note: DB2015V SPI SLAVE BUS Application Notes.		

4.2 Zero Cross Circuits

SECC may use Zero Cross function to synchronize others PLC device for bandwidth managements.

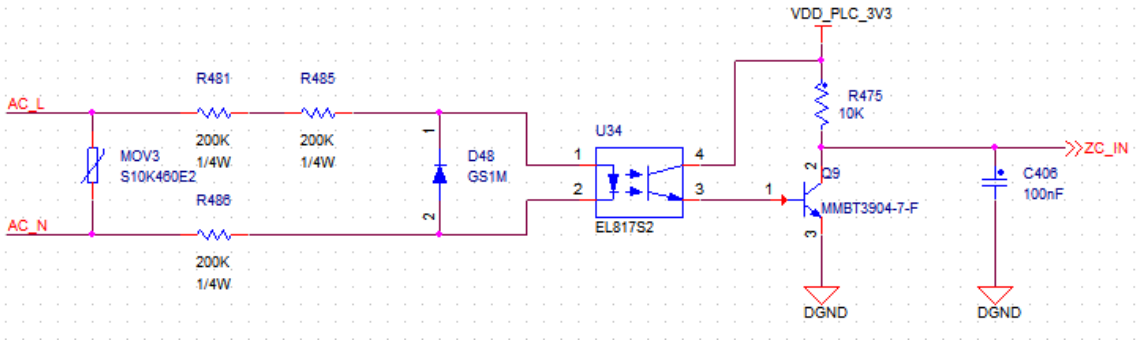


Figure 7: HPGP Zero Cross Circuits

Note: AC line zero cross detection requires an external optical coupler and filter circuits.

4.3 LED Usage

The GPIO [3] is pre-configured as Output to drive extern LED. The LED circuit is recommended as Figure-7. While the HPGP connection is setup, the low level is set on GPIO [3] pin, the LED is lighted.

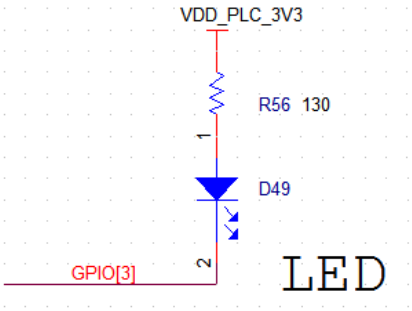


Figure 8: GPIO [3] Recommended Circuits

4.4 HPGP Coupler

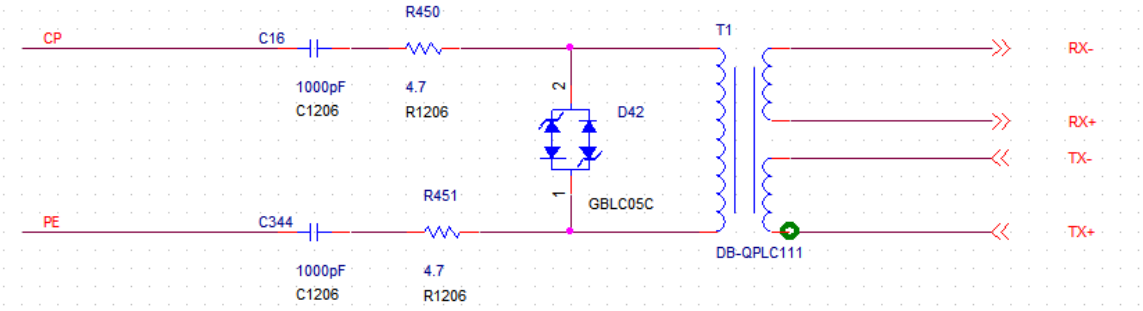


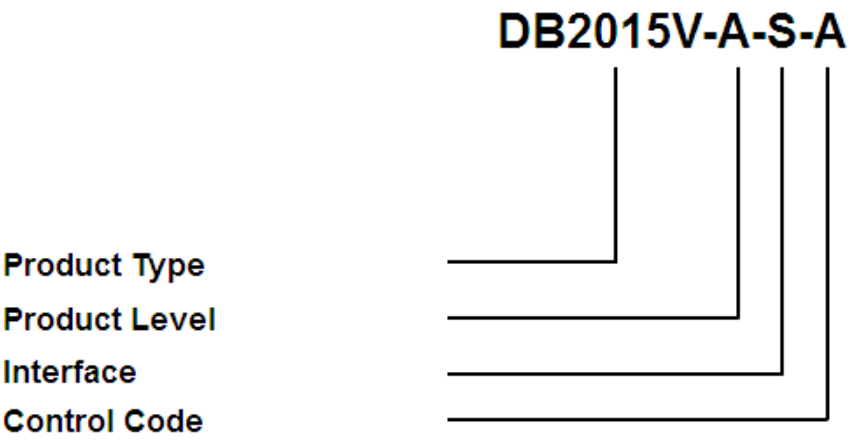
Figure 9: HPGP Coupler Circuit

Two coupling capacitors block the DC voltages present on the pilot wire. The component values may change after component optimization.
A 1:1:1 turn ratio transformer and two 4.7 Ω series resistors limit transient current and set the output impedance to about 6 Ω. These current limiting resistor values may be adjusted slightly to trim the transmitter voltage output amplitude.
A TVS diode is placed between the DC blocking capacitors and isolation resistors and the PLC coupling transformer to isolate from the second stage circuitry and clamp the surge voltage to a more acceptable level for the DB2015V module.

Recommended Coupler-Transformer

Part No.	Vendor	Features	Description
DB-QPLC111	Dropbeats	Industrial	SECC Application
HMU1230NL	Pulse	AEC-Q200 Grade 1	EVCC Application

5 ORDER INFORMATION



Product Type	Product Level	Interface	Control Code
DB2015V	A: Automotive I: Industrial	S: SPI	……

Order Code	Chipset	Temperature Range	Interface	Applications
DB2015V-I-S-B	QCA7000-AL3B	-40 – 85^{0}C	SPI	Industrial EVSE
DB2015V-A-S-B	QCA7005-AL33	-40 – 105^{0}C	SPI	Automotive EV