TobuFi is an advanced SOM (system on module) built using the cutting-edge Qualcomm® QCS405 chip and a high-end dual-band Wi-Fi 6 radio powered by QCN9074 chipset.
With an additional WiFi 6 radio, AI and DSP features integrated into the QCS405, TobuFi ensures reliable data transmission and efficient processing that are ideal for robotics and drone applications. Its secondary WiFi radio provides additional versatility and flexibility for development. TobuFi's interface-rich design offers straightforward integration, while high-end radio supports narrow channels, extended frequency range, and frequency shifting with non-standard center frequencies is ideal for long-range communication even in very noisy environments.

Quick specs

- Processor based on Qualcomm QCS405 SoC;
- Radio 1 based on Qualcomm QCN9074 Wi Fi 6 (802.11a/g/n/ac/ax), available in two versions: 2.4 GHz + 5 GHz or 2.4 GHz + 6 GHz; supports single band operation (2.4 GHz or 5 GHz/6 GHz, non concurrent) with 2×4 configuration;
- Extended operating frequency ranges (preliminary): 2360–3150 MHz for 2.4 GHz band operation, 4550–6630 MHz for 5 GHz band operation, 5325–7495 MHz for 6 GHz band operation. These values are based on initial validation data and remain subject to further optimization. Ranges may be extended in future revisions;
- Support for narrow bandwidth 5/10MHz with standard 20/40/80/160 MHz in full extended range;
- Optimized for reliable long-range communication (10+ km wireless links);
- Frequency tuning resolution of 1 MHz for extended frequency operation: 2.4 GHz and 5 GHz/6 GHz;
- Non-standard center frequency channels for interference mitigation;
- Radio 2 based on Qualcomm WCN3980 Wi-Fi 5 (802.11a/g/n/ac) 2.4 GHz or 5 GHz with 1x1 MU-MIMO 20/40/80 MHz;
- Radio 1:
  Option 1 | 2.4 GHz up to 29dBm; 5 GHz 26dBm RF output power per chain;
  Option 2 | 2.4 GHz up to 29dBm; 6 GHz 26dBm RF output power per chain;
- Radio 2 | 2.4 GHz up to 16dBm; 5 GHz 16dBm RF output power per chain;
- Memory eMCP: LPDDR3 1GB + eMMC 8GB;
- LGA; size – 36.6 by 76.6 mm;
- Software platform: OpenEmbedded / Yocto;
- Available interfaces: USB 3.0; USB 2.0; RGMI; DSI, HDMI; I2S; DMIC; SDC; UART; SPI; I2C; GPIO.

Table of Contents

1. Features

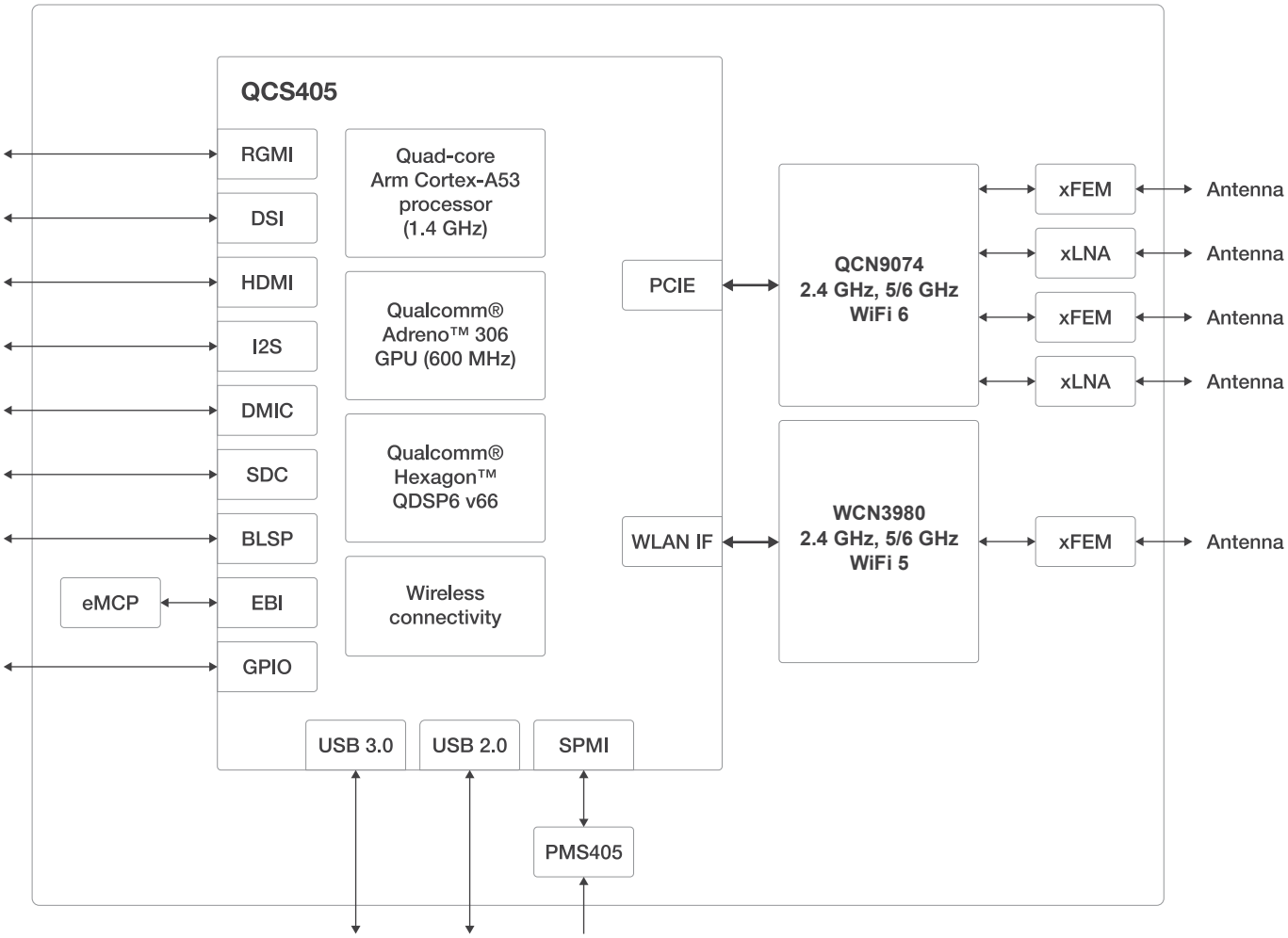
TABLE 1-1. TOBUFI FEATURES

Feature list	Description
CPU	Qualcomm QCS405 Arm Cortex A53 quad-core; 1.4GHz; 64-bit
Memory	LPDDR3 1GB + eMMC 8GB
Graphics	Qualcomm® Adreno™ 306 graphics processing unit (GPU) with 64-bit addressing; 600MHz
DSP	Qualcomm® Hexagon™ QDSP6 v66 with Low Power Island and Voice accelerators
Audio	Serial low-power interchip media bus (SLIMbus); MI2S
Display	General display interfaces: One 4-lane MIPI DSI ports, DSI support up to 720P, HDMIv1.4a support up to 1080p 30fps, RGB support, SPI
WIFI	Qualcomm QCN9074 Wi Fi 6 (802.11a/g/n/ac/ax), operating on either 2.4 GHz or 5/6 GHz, with 2×4 (2 transmit chains and 4 receive chains) MU MIMO, 20/40/80/160 MHz; 2.4 GHz up to 29 dBm, 5/6 GHz up to 26 dBm RF output power per chain; Qualcomm WCN3980 Wi-Fi 5 (802.11a/g/n/ac), operating on either 2.4 GHz or 5 GHz with 1x1 MU-MIMO 20/40/80 2.4 GHz up to 16dBm; 5 GHz 16dBm RF output power per chain
USB	USB 2.0, USB 3.0
Ethernet	RGMI
SD	One 8-bit (SDC1, 1.8 V) and one 4-bit (SDC2, 1.8/2.95 V)
Other interfaces	I2S; DMIC; SDC; UART; SPI; I2C; GPIO
Size	36.6 x 76.6 mm
Module type	LGA

2. Block diagram

The following figure provides a basic overview of the TobuFi SoM.

FIGURE 2-1. BLOCK DIAGRAM



3. Module pinout and Pin description

FIGURE 3-1. PIN ASSIGNMENTS

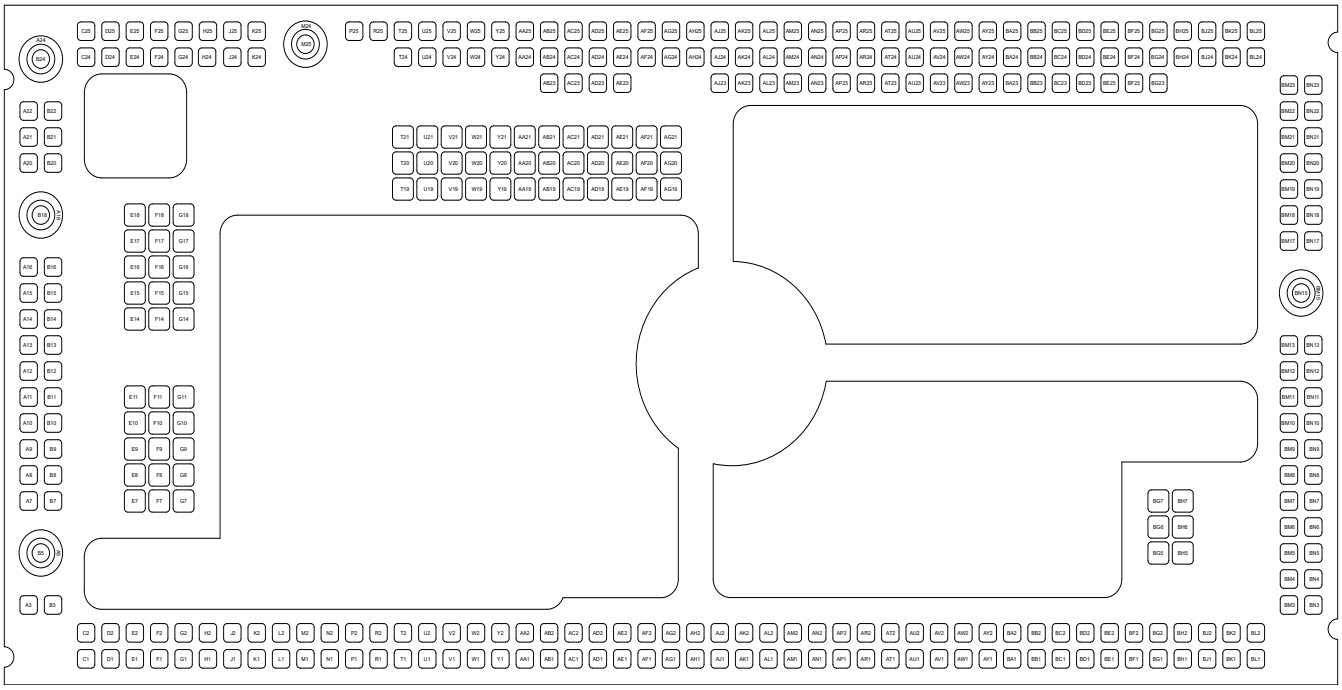


TABLE 3-1. I/O DESCRIPTION (PAD TYPE) PARAMETERS

Symbol	Description
AI	Analog input
AO	Analog output
DI	Digital input
DO	Digital output
DIO	Digital bidirectional
B	Digital bidirectional (direction changes dynamically)
PI	Power input
PO	Power ouput
GND	Ground
RF In/Out	RF input/output
Z	High-impedance
NC	Not connected
PD	Internal pull-down resistor (enabled by default)
PU	Internal pull-up resistor (enabled by default)

TABLE 3-2. POWER, GROUND AND RESET

Pin ID	Pin name	Type	Description
AU1, AU2, AV1, AV2, AW2, AY2	3V3	PI	3.3V power supply
F1, G1, G2, H2, J2	5V_LNA	PI	5V power supply for LNA
J1, K1, K2, L1, L2	5V_XPA	PI	5V power supply for XPA
N1, N2, P1, P2	1V8_OUT	PO	1.8V output voltage
A10, A11, A12, A15, A16, A18, A20, A21, A22, A24, A3, A5, A7, AA1, AA19, AA20, AA2, AA21, AB19, AB20, AB21, AC1, AC19, AC20, AC2, AC21, AD19, AD20, AD21, AE1, AE19, AE20, AE21, AE24, AE25, AF19, AF20, AF21, AG1, AG19, AG20, AG2, AG21, AG25, AH24, AH25, AJ1, AJ2, AJ23, AK23, AL1, AL2, AL23, AM23, AN1, AN23, AP24, AP25, AW1, AY1, B10, B11, B12, B3, BE1, BG5, BG6, BG7, BH5, BH6, BH7, BM10, BM13, BM15, BN7, C2, C24, C25, D2, E10, E1, E11, E14, E15, E16, E17, E18, E2, E7, E8, E9, F10, F11, F14, F15, F16, F17, F18, F2, F25, F7, F8, F9, G10, G11, G14, G15, G16, G17, G18, G25, G7, G8, G9, H1, H25, J25, K25, M1, M2, M24, P25, R1, R2, R25, T19, T20, T21, U1, U19, U20, U2, U21, V19, V20, V21, V24, V25, W1, W19, W20, W2, W21, Y19, Y20, Y21	GND	GND	Ground
B7, B8, B9, B13, B14, B15, B16, B20, B21, B22, BG1, BG2, BH1, BH2, BJ1, BJ2, BK1, BK2, BL1, BL2, BM3, BN4, D24, E24, F24, G24, H24, J24, K24	NC	NC	Not connected
BN5	QCS_RESIN_N	DO	Power reset
BB2	KPD_PWR_N	DO	Power-on trigger (active low)
BB1	PON_1	DI	Start-up trigger

TABLE 3-3. RADIO

Pin ID	Pin name	Type	Description
M25	RXTX_CH0	RF In/Out	Chain0 Transmitter/Receiver line for antenna
B24	RX_CH1	RF In	Chain1 Receiver line for antenna
B18	RXTX_CH2	RF In/Out	Chain2 Transmitter/Receiver line for antenna
B5	RX_CH3	RF In	Chain3 Receiver line for antenna
BN15	RXTX_CH4	RF In/Out	Chain4 Transmitter/Receiver line for antenna a
U24	2G_PA_EN_CH0	AI	Chain0 2.4GHz XPA enable
U25	5G_PA_EN_CH0	AI	Chain0 5GHz XPA enable
T24	2G_LNA_EN_CH0	AI	Chain0 2.4GHz LNA enable
T25	5G_LNA_EN_CH0	AI	Chain0 5GHz LNA enable
E25	2G_LNA_EN_CH1	AI	Chain1 2.4GHz LNA enable
D25	5G_LNA_EN_CH1_5V	AI	Chain1 5GHz LNA enable
A14	2G_PA_EN_CH2	AI	Chain2 2.4GHz XPA enable
A9	5G_PA_EN_CH2	AI	Chain2 5GHz XPA enable
A13	2G_LNA_EN_CH2	AI	Chain2 2.4GHz LNA enable
A8	5G_LNA_EN_CH2	AI	Chain2 5GHz LNA enable
C1	2G_LNA_EN_CH3	AI	Chain3 2.4GHz LNA enable
D1	5G_LNA_EN_CH3_5V	AI	Chain3 5GHz LNA enable

TABLE 3-4. USB 3.0

Pin ID	Pin name	Type	Description
AN2	USB1_HS_VBUS	DI	USB HS data bus voltage (5V)
AH1	USB1_HS_D_P	AI, AO	USB HS data positive
AH2	USB1_HS_D_N	AI, AO	USB HS data negative
BC1	USB1_HS_ID	AI	USB1 HS ID
AM2	USB0_SSRX_D_P	AI	USB SS receive data positive
AM1	USB0_SSRX_D_N	AI	USB SS receive data negative
AK1	USB0_SSTX_L1XY_D_P	AO	USB SS transmit data positive
AK2	USB0_SSTX_L1XY_D_N	AO	USB SS transmit data negative

TABLE 3-5. USB 2.0

Pin ID	Pin name	Type	Description
AE2	USB0_HS_VBUS	DI	USB HS data bus voltage (5V)
AF1	USB0_HS_D_P	AI, AO	USB HS data positive
AF2	USB0_HS_D_N	AI, AO	USB HS data negative
BC2	USB0_HS_ID	AI	USB0 HS ID

TABLE 3-6. SD CARD

Pin ID	Pin name	Type	Description
AR1	SDC2_CLK	DI	Clock
AR2	SDC2_CMD	DIO	Command line
AP2	SDC2_DATA_0	AI, AO	Data Line 0
AP1	SDC2_DATA_1	AI, AO	Data Line 1
AT2	SDC2_DATA_2	AI, AO	Data Line 2
AT1	SDC_DATA_3	AI, AO	Data Line 3

TABLE 3-7. MIPI

Pin ID	Pin name	Type	Description
AL25	MIPI_DSI0_CLK_N	AO	MIPI display serial interface 0 clock negative
AL24	MIPI_DSI0_CLK_P	AO	MIPI display serial interface 0 clock positive
AN24	MIPI_DSI0_LANE0_P	AI, AO	MIPI display serial interface 0 lane 0 positive
AN25	MIPI_DSI0_LANE0_N	AI, AO	MIPI display serial interface 0 lane 0 negative
AM24	MIPI_DSI0_LANE1_P	AI, AO	MIPI display serial interface 0 lane 1 positive
AM25	MIPI_DSI0_LANE1_N	AI, AO	MIPI display serial interface 0 lane 1 negative
AK24	MIPI_DSI0_LANE2_P	AI, AO	MIPI display serial interface 0 lane 2 positive
AK25	MIPI_DSI0_LANE2_N	AI, AO	MIPI display serial interface 0 lane 2 negative
AJ24	MIPI_DSI0_LANE3_P	AI, AO	MIPI display serial interface 0 lane 3 positive
AJ25	MIPI_DSI0_LANE3_N	AI, AO	MIPI display serial interface 0 lane 3 negative

TABLE 3-8. HDMI

Pin ID	Pin name	Type	Description
AF24	HDMI_ARC_P	DI	HDMI ARC input different pair positive
AF25	HDMI_ARC_N	DI	HDMI ARC input different pair negative
Y1	HDMI_TX_TMDS_TCLK_N	DI	HDMI clock negative
Y2	HDMI_TX_TMDS_TCLK_P	DI	HDMI clock positive
AD1	HDMI_TX_TMDS_TX0_N	DO	HDMI TMDS data 0 negative
AD2	HDMI_TX_TMDS_TX0_P	DO	HDMI TMDS data 0 positive
V1	HDMI_TX_TMDS_TX1_N	DO	HDMI TMDS data 1 negative
V2	HDMI_TX_TMDS_TX1_P	DO	HDMI TMDS data 1 positive
AB1	HDMI_TX_TMDS_TX2_N	DO	HDMI TMDS data 2 negative
AB2	HDMI_TX_TMDS_TX2_P	DO	HDMI TMDS data 2 positive

TABLE 3-9. JTAG

Pin ID	Pin name	Type	Description
BN13	QCS_JTAG_TCK	DI	JTAG Clock Input
BN12	QCS_JTAG_TMS	B	JTAG Mode-select Input
BM12	QCS_JTAG_TDI	DI	JTAG Data Input
BM11	QCS_JTAG_TRST_N	DI	JTAG Reset
BN11	QCS_JTAG_TDO	DO	JTAG Data Out
BN10	JTAG_SRST_N	DI	JTAG Reset for Debug

TABLE 3-10. COEX

Pin ID	Pin name	Type	Description
BF23	COEX_CLK	DI	WLAN COEX Clock input
BG24	COEX_DATA	B	WLAN COEX Data input/output
BH24	COEX_RXD	DI	WLAN COEX Receiver
BJ24	COEX_TXD	DO	WLAN COEX Transmitter

TABLE 3-11. UART

Pin ID	Pin name	Type	Description
AB25	GPIO_39_BLSP2_UART_TX_B	DO	CPU UART Transmitter
AB24	GPIO_40_BLSP2_UART_RX_B	DI	CPU UART Receiver
BN9	GPIO_17_BLSP2_UART_TX	DO	CPU UART Transmitter
BM9	GPIO_18_BLSP2_UART_RX	DI	CPU UART Receiver
BM6	GPIO_22_BLSP1_UART_TX	DO	CPU UART Transmitter
BN6	GPIO_23_BLSP1_UART_RX	DI	CPU UART Receiver
BA1	GPIO_30_BLSP0_UART_TX	DO	CPU UART Transmitter
BA2	GPIO_31_BLSP0_UART_RX	DI	CPU UART Receiver
T2	QCN_GPIO48_DEBUG_UART_TXD	DO	Radio UART Transmitter
T1	QCN_GPIO49_DEBUG_UART_RXD	DI	Radio UART Receiver

TABLE 3-12. I2C

Pin ID	Pin name	Type	Description
BN8	GPIO_19_BLSP2_I2C_SDA	B	I2C Data line
BM7	GPIO_20_BLSP2_I2C_SCL	AI	I2C Clock line
BM4	GPIO_24_BLSP1_I2C_SDA	B	I2C Data line
BM5	GPIO_25_BLSP1_I2C_SCL	AI	I2C Clock line

TABLE 3-13. RCA/OPTICAL

Pin ID	Pin name	Type	Description
AG24	SPDIFRX_COAX	AI	Coax receiver line
BB25	LPI_GPIO_6/SPDIF_TX_COAX	AO	Coax transmitter line
AT23	GPIO_119/SPDIF_OPTICAL_RX	AI	Optical receiver line

TABLE 3-14. RGMII

Pin ID	Pin name	Type	Description
BM22	GPIO_63	AO	RGMII CK Transmitter
BM23	GPIO_64	AO	RGMII Transmitter 3
BM21	GPIO_65	AO	RGMII Transmitter 2
BN23	GPIO_66	AO	RGMII Transmitter 1
BM18	GPIO_67	AO	RGMII Transmitter 0
BN20	GPIO_68	AO	RGMII CTL Transmitter
BN21	GPIO_69	AI	RGMII CK Receiver

Pin ID	Pin name	Type	Description
BN22	GPIO_70	AI	RGMII Receiver 3
BM19	GPIO_71	AI	RGMII Receiver 2
BM20	GPIO_72	AI	RGMII Receiver 1
BN18	GPIO_73	AI	RGMII Receiver 0
BN19	GPIO_74	AI	RGMII CTL Receiver
BM17	GPIO_75	IO	RGMII MDIO
BN17	GPIO_76	AO	RGMII MDC

TABLE 3-15. LPI GPIO

Pad #	Pad Name	Voltage	Type	Function	Functional Description
AY25	LPI_GPIO_1	LPI	PD	Ext_mclk3	External MCLK
				Aud_ref_clk1	Audio Reference Clock1 (44.1K Family)
BA25	LPI_GPIO_2	LPI	PD	Lpi_aud_sb_clk	Audio SLIMbus Clock
				Lpi_i2s_6_sck	I2S6 Clock f (Codec Attach)
AW24	LPI_GPIO_3	LPI	PD	Lpi_aud_sb_data0	Audio SLIMbus Data0
				Lpi_i2s_6_ws	I2S6 WS (Codec Attach)
AW23	LPI_GPIO_4	LPI	PD	Lpi_aud_sb_data1	Audio SLIMbus Data1
				Lpi_i2s_6_data0	I2S6 Data0 (Codec Attach)
AY24	LPI_GPIO_5	LPI	PD	Lpi_wsa_clk	Sound wire interface clock
				Ext_mclk4	External MCLK4
				Aud_ref_clk2	Audio reference clock2 (48K Family)
				Lpi_aud_sb_data2	Audio SLIMbus Data2
				Lpi_i2s_6_data1	I2S6 Data1 (Codec Attach)
AY23	LPI_GPIO_20	LPI	PD	Lpi_wsa_data	Sound wire interface data

TABLE 3-16. GPIO

Pad #	Pad Name	Voltage	Type	Alt function	Functional Description
BN3	GPIO_08	1.8V	DO	1	PMS_MCLK
BE2	GPIO_14	1.8V	PD	1	hdmi_tx_cec
BD2	GPIO_15	1.8V	PU	1	Hdmi_ddc_clk
BD1	GPIO_16	1.8V	PU	1	Hdmi_ddc_data
BN9	GPIO_17	1.8V	PD	1	blsp_uart_tx_a[2] (firmware-assigned)
				2	blsp_spi_mosi[2]
BM9	GPIO_18	1.8V	PD	1	blsp_uart_rx_a[2] (firmware-assigned)
				2	blsp_spi_miso[2]

Pad #	Pad Name	Voltage	Type	Alt function	Functional Description
BN8	GPIO_19	1.8V	PD	1	blsp_uart_cts_n[2]
				2	aud_cdc_int2
				3	blsp_i2c_sda_a[2] (firmware-assigned)
				4	blsp_spi_cs_n[2]
BM7	GPIO_20	1.8V	PD	1	blsp_uart_rfr_n[2]
				2	aud_cdc_int1
				3	blsp_i2c_scl_a[2] (firmware-assigned)
				4	blsp_spi_clk[2]
BM6	GPIO_22	1.8V	PD	1	blsp_uart_tx[1] (firmware-assigned)
				2	blsp_spi_mosi_a[1]
				3	asdiv1
BN6	GPIO_23	1.8V	PD	1	blsp_uart_rx[1] (firmware-assigned)
				2	blsp_spi_miso_a[1]
				3	asdiv2
BM4	GPIO_24	1.8V	PD	1	blsp_uart_cts_n[1]
				2	blsp_i2c_sda[1] (firmware-assigned)
				3	blsp_spi_cs_n_a[1]
BM5	GPIO_25	1.8V	PD	1	blsp_uart_rfr_n[1]
				2	blsp_i2c_scl[1] (firmware-assigned)
				3	blsp_spi_clk_a[1]
W25	GPIO_26	1.8V	PD	1	Rgb_data_r[0]
				2	Blsp_uart_tx[5]
				3	Blsp_spi_mosi[5] (SPI NOR boot is support)
AB23	GPIO_27	1.8V	PD	1	Rgb_data_r[1]
				2	Blsp_uart_rx[5]
				3	Blsp_spi_mosi[5] (SPI NOR boot is supported)
W24	GPIO_28	1.8V	PD	1	Rgb_data_r[2]
				2	Blsp_uart_cts_n[5]
				3	Blsp_i2c_sda[5]
				4	Blsp_spi_cs_n[t] (SPI NOR boot is supported)
				5	Gcc_gp1_clk_b
AR25	GPIO_29	1.8V	PD	1	Rgb_data_r[3]
				2	Blsp_uart_rfr_n[5]
				3	Blsp_i2c_scl[5]
				4	Blsp_spi_clk[5] (SPI NOR boot is supported)
				5	Gcc_gp2_clk_b
BA1	GPIO_30	1.8V	PD	1	Blsp_spi_mosi[0]
				2	Blsp_uart_tx[0] (firmware-assigned)
				3	Gcc_gp3_clk_b

Pad #	Pad Name	Voltage	Type	Alt function	Functional Description
BA2	GPIO_31	1.8V	PD	1	Blsp_spi_miso[0]
				2	Blsp_uart_rx[0] (firmware-assigned)
BF2	GPIO_32	1.8V	PD	1	Blsp_spi_cs_n[0]
				2	Blsp_uart_cts_n[0]
				3	Blsp_i2c_sda[0]
BF1	GPIO_33	1.8V	PD	1	Blsp_spi_clk[0]
				2	Blsp_uart_rfr_n[0]
				3	Blsp_i2c_scl[0]
BM8	GPIO_36	1.8V	PD	1	Asdiv1_mir
AB25	GPIO_39	1.8V	PD	1	Rgb_data_r[4]
				2	Spi_lcd_dc
				3	Blsp_uart_tx_b[2] (firmware-assigned)
				4	Gcc_gp3_clk_a
AB24	GPIO_40	1.8V	PD	1	Rgb_data_r[5]
				2	Spi_lcd_bl_pwm
				3	Blsp_uart_rx_b[2] (firmware-assigned)
				4	Gp_pdm_1a
AD25	GPIO_41	1.8V	PD	1	Rgb_data_g[0]
				2	Blsp_i2c_sda_b[2]
				3	Gp0_clk
AD24	GPIO_42	1.8V	PD	1	Rgb_data_g[1]
				2	Blsp_i2c_scl_b[2]
				3	Gp1_clk
AT25	GPIO_43	1.8V	PD	1	Rgb_data_g[2]
				2	Pwm_led11
				3	Gp_pdm_0b
AR24	GPIO_44	1.8V	PD	1	Rgb_data_g[3]
				2	Pwm_led12
				3	Blsp_spi_cs1_n[5]
AC23	GPIO_45	1.8V	PD	1	Rgb_data_g[4]
				2	Pwm_led13
				3	Blsp_spi_cs2_np[5]
AD23	GPIO_46	1.8V	PD	1	Rgb_data_g[5]
				2	Pwm_led14
				3	Blsp_spi_cs3_n[5]
Y24	GPIO_47	1.8V	PD	1	Rgb_data_b[0]
				2	Pwm_led15
				3	Blsp_spi_mosi_bp[1]

Pad #	Pad Name	Voltage	Type	Alt function	Functional Description
Y25	GPIO_48	1.8V	PD	1	Rgb_data_b[1]
				2	Pwm_led16
				3	Blsp_spi_miso_b[1]
				4	Gp_pdm_2a
AA24	GPIO_49	1.8V	PD	1	Rgb_data_b[2]
				2	Pwm_led17
				3	Blsp_spi_cs_n_b[1]
				4	Gp_pdm_2b
AU25	GPIO_50	1.8V	PD	1	Rgb_data_b[3]
				2	Pwm_led18
				3	Blsp_spi_clk_b[1]
AV25	GPIO_51	1.8V	PD	1	Rgb_data_b[4]
				2	Pwm_led19
				3	Ext_mclk1_b
AA25	GPIO_52	1.8V	PD	1	Rgb_data_b[5]
				2	Pwm_led20
				4	I2s_3_sck_b
				5	Ldo_update
AW25	GPIO_53	1.8V	PD	1	Rgb_hsync
				2	Pwm_led21
				3	I2s_3_ws_b
AT24	GPIO_54	1.8V	PD	1	Rgb_vsync
				2	I2s_3_data0_b
				3	Ldo_en
AE23	GPIO_55	1.8V	PD	1	Rgb_de
				2	I2s_3_data1_b
				3	Gp_pdm_0a
AP23	GPIO_56	1.8V	PD	1	Rgb_clk
				3	I2s_3_data2_b
AR23	GPIO_57	1.8V	PD	1	Rgb_mdp_vsync_p
				3	I2s_3_data3_b
AC25	GPIO_58	1.8V	PD	1	Rgb_data_b[6]
				2	Gp_pdm_1b
AV24	GPIO_59	1.8V	PD	1	Rgb_data_b[7]
AC24	GPIO_78	1.8V	PD	1	Rgb_data_g[6]
AU23	GPIO_79	1.8V	PD	1	Rgb_data_g[7]
AU24	GPIO_80	1.8V	PD	1	Rgb_data_r[6]
AV23	GPIO_81	1.8V	PD	1	Rgb_data_r[7]

Pad #	Pad Name	Voltage	Type	Alt function	Functional Description
BB24	GPIO_87	1.8V	PD	1	I2s_1_sck
				2	Dsd_clk_a
BA24	GPIO_88	1.8V	PD	1	I2s_1_ws
				2	I2s_1_data0_dsd0
BD25	GPIO_89	1.8V	PD	1	I2s_1_data0
				2	I2s_1_data0_dsd1
BC25	GPIO_90	1.8V	PD	1	I2s_1_data1
				2	I2s_1_data2_dsd2
BA23	GPIO_91	1.8V	PD	1	I2s_1_data2
				2	I2s_1_data3_dsd3
BB23	GPIO_92	1.8V	PD	1	I2s_1_data3
				2	I2s_1_data4_dsd4
BC24	GPIO_93	1.8V	PD	1	I2s_1_data4
				2	Pwm_led22
				3	I2s_1_data5_dsd5
BH25	GPIO_94	1.8V	PD	1	I2s_1_data5
				2	Pwm_led23
				3	I2s_1_data6_mir
BK25	GPIO_95	1.8V	PD	1	I2s_1_data6
				2	Pwm_led1
				3	I2s_1_data7_mir
BG25	GPIO_96	1.8V	PD	1	I2s_1_data7
				2	Pwm_led2
BJ25	GPIO_97	1.8 V, 3.15 V	PD	1	I2s_2_sck
BD24	GPIO_103	1.8V	PD	1	Ext_mclk1_a
				2	Mclk_in2
BL25	GPIO_104	1.8V	PD	1	I2s_3_sck_a
BL24	GPIO_105	1.8V	PD	1	I2s_3_ws_a
BK24	GPIO_106	1.8V	PD	1	I2s_3_data0_a
				2	Ebi2_lcd_rs_n
				3	Hdmi_hot_plug_mir
BE24	GPIO_107	1.8V	PD	1	I2s_3_data1_a
				2	Ebi2_lcd_cs_n
BE25	GPIO_108	1.8V	PD	1	I2s_3_data2_a
				2	Ebi2_lcd_te
				4	Pwm_led3

Pad #	Pad Name	Voltage	Type	Alt function	Functional Description
BF25	GPIO_109	1.8V	PD	1	I2s_3_data3_a
				2	Ebi2_lcd_en_n
				3	Pwm_led4
BF24	GPIO_110	1.8V	PD	1	I2s_4_sck
				2	Ebi2_a_d_8
				3	Dsd_clk_b
				4	Pwm_led5
BE23	GPIO_111	1.8V	PD	1	I2s_4_ws
				2	I2s_4_data0_dsd0
				3	Pwm_led6
BC23	GPIO_112	1.8V	PD	1	I2s_4_data_0
				2	I2s_4_data1_dsd1
				3	Pwm_led7
BD23	GPIO_113	1.8V	PD	1	I2s_4_data_1
				2	I2s_4_data2_dsd2
				3	Pwm_led8
BG23	GPIO_116	1.8V	PD	1	i2s_4_data5_dsd5
				2	spkr_dac0

NOTE: All listed alternative functions are supported by hardware. The function pre-selected in firmware is marked (firmware-assigned) and must not be changed without prior agreement, as it is required for core system operation.

TABLE 3-17. PIN STATUS ON BOOT

Pin name	Pin name	Voltage	Functional Description
FORCED_USB_BOOT	GPIO_45	1.8 V	Forced USB boot; Configurable I/O
BOOT_CONFIG_0	GPIO_55	1.8 V	Fast_boot_select bit 0; Configurable I/O
BOOT_CONFIG_1	GPIO_56	1.8 V	Fast_boot_select bit 1; Configurable I/O
BOOT_CONFIG_2	GPIO_57	1.8 V	Fast_boot_select bit 2; Configurable I/O
BOOT_CONFIG_3	GPIO_49	1.8 V	Fast_boot_select bit 3; Configurable I/O
BOOT_CONFIG_4	GPIO_54	1.8 V	Fast_boot_select bit 4; Configurable I/O
BOOT_CONFIG_5	GPIO_52	1.8 V	Fast_boot_select bit 5; Configurable I/O
BOOT_CONFIG_6	GPIO_51	1.8 V	Fast_boot_select bit 6; Configurable I/O
BOOT_CONFIG_7	GPIO_48	1.8 V	Fast_boot_select bit 7; Configurable I/O
BOOT_CONFIG_8	GPIO_59	1.8 V	Fast_boot_select bit 8; Configurable I/O
BOOT_CONFIG_9	GPIO_46	1.8 V	Fast_boot_select bit 9; Configurable I/O
BOOT_CONFIG_10	GPIO_79	1.8 V	Fast_boot_select bit 10; Configurable I/O
BOOT_CONFIG_11	GPIO_78	1.8 V	Fast_boot_select bit 11; Configurable I/O
BOOT_CONFIG_12	GPIO_47	1.8 V	Fast_boot_select bit 12; Configurable I/O
BOOT_CONFIG_13	GPIO_50	1.8 V	Fast_boot_select bit 13; Configurable I/O
BOOT_CONFIG_14	GPIO_80	1.8 V	Fast_boot_select bit 14; Configurable I/O

NOTE: These pins are for boot configuration, use them cautiously

4. Electrical characteristics

TABLE 4-1. POWER SUPPLY DC CHARACTERISTICS

Symbol	Parameter	Minimum	Typical	Maximum	Units
DVDD33	3.3V Supply Voltage	3.13	3.3	3.46	V

TABLE 4-2. TEMPERATURE LIMIT RATINGS

Parameter	Minimum	Maximum	Units
Storage Temperature (Commercial)	-40	+70	°C
Storage Temperature (Industrial)	-40	+90	°C
Commercial Operating Temperature	0	+65	°C
Industrial Operating Temperature	-40	+85	°C
Humidity	10	90	%RH
Storage humidity	5	90	%RH

5. Power management

TABLE 5-1. POWER CONSUMPTION

Scenario		Rate	Current	Total power
Throughput with iperf and 95% CPU load, 2x2				

6. Radio characteristics

2.4 GHZ 802.1AX 20 MHZ, QCN RADIO

	MCS0	MCS1	MCS2	MCS3	MCS4	MCS5	MCS6	MCS7	MCS8	MCS9	MCS10	MCS11
Data rate TX (Mbps)	17.2	34.4	51.6	68.8	103.2	137.6	154.9	172.1	206.5	229.4	258.1	286.8
TX power (dBm)												
Data rate RX (Mbps)	34.4	68.8	103.2	137.6	206.5	275.3	309.7	344.1	412.9	458.8	516.2	573.5
RX sensitivity (dB)												

2.4 GHZ 802.1AX 40 MHZ, QCN RADIO

	MCS0	MCS1	MCS2	MCS3	MCS4	MCS5	MCS6	MCS7	MCS8	MCS9	MCS10	MCS11
Data rate TX (Mbps)	34.4	68.8	103.2	137.6	206.5	275.3	309.7	344.1	412.9	458.8	516.2	573.5
TX power (dBm)												
Data rate RX (Mbps)	68.8	137.6	206.5	275.3	412.9	550.6	649.4	688.2	825.9	917.6	1032.4	1147.1
RX sensitivity (dB)												

5GHZ 802.11AX 20 MHZ, QCN RADIO

	MCS0	MCS1	MCS2	MCS3	MCS4	MCS5	MCS6	MCS7	MCS8	MCS9	MCS10	MCS11
Data rate TX (Mbps)	72.1	144.1	216.2	288.2	432.4	576.5	648.5	720.6	864.7	960.8	1080.9	1201
TX power (dBm)												
Data rate RX (Mbps)	34.4	68.8	103.2	137.6	206.5	275.3	309.7	344.1	412.9	458.8	516.2	573.5
RX sensitivity (dB)												

5GHZ 802.11AX 40 MHZ, QCN RADIO

	MCS0	MCS1	MCS2	MCS3	MCS4	MCS5	MCS6	MCS7	MCS8	MCS9	MCS10	MCS11
Data rate TX (Mbps)	72.1	144.1	216.2	288.2	432.4	576.5	648.5	720.6	864.7	960.8	1080.9	1201
TX power (dBm)												
Data rate RX (Mbps)	68.8	137.6	206.5	275.3	412.9	550.6	649.4	688.2	825.9	917.6	1032.4	1147.1
RX sensitivity (dB)												

5GHZ 802.11AX 80 MHZ, QCN RADIO

	MCS0	MCS1	MCS2	MCS3	MCS4	MCS5	MCS6	MCS7	MCS8	MCS9	MCS10	MCS11
Data rate TX (Mbps)	72.1	144.1	216.2	288.2	432.4	576.5	648.5	720.6	864.7	960.8	1080.9	1201
TX power (dBm)												
Data rate RX (Mbps)	144.1	288.2	432.4	576.5	864.7	1152.9	1297.1	1441.2	1729.4	1921.6	2161.8	2402
RX sensitivity (dB)												

5GHZ 802.11AX 160 MHZ, QCN RADIO

	MCS0	MCS1	MCS2	MCS3	MCS4	MCS5	MCS6	MCS7	MCS8	MCS9	MCS10	MCS11
Data rate TX (Mbps)	72.1	144.1	216.2	288.2	432.4	576.5	648.5	720.6	864.7	960.8	1080.9	1201
TX power (dBm)												
Data rate RX (Mbps)	288.2	256.5	864.7	1152.9	1729.4	2305.9	2594.1	2882.4	3458.8	3843.1	4323.5	4803.9
RX sensitivity (dB)												

2.4 GHZ 802.1AC 20 MHZ, WCN RADIO

	MCS0	MCS1	MCS2	MCS3	MCS4	MCS5	MCS6	MCS7	MCS8
Data rate (Mbps)	7.2	14.4	21.7	28.9	43.3	57.8	65	72.2	86.7
TX power (dBm)									
RX sensitivity (dB)									

2.4 GHZ 802.1AC 40 MHZ, WCN RADIO

	MCS0	MCS1	MCS2	MCS3	MCS4	MCS5	MCS6	MCS7	MCS8	
Data rate (Mbps)	15	30	45	60	90	120	135	150	180	200
TX power (dBm)										
RX sensitivity (dB)										

5GHZ 802.11AC 20 MHZ, WCN RADIO

	MCS0	MCS1	MCS2	MCS3	MCS4	MCS5	MCS6	MCS7	MCS8
Data rate (Mbps)	7.2	14.4	21.7	28.9	43.3	57.8	65	72.2	86.7
TX power (dBm)									
RX sensitivity (dB)									

5GHZ 802.11AC 40 MHZ, WCN RADIO

	MCS0	MCS1	MCS2	MCS3	MCS4	MCS5	MCS6	MCS7	MCS8	MCS9
Data rate (Mbps)	15	30	45	60	90	120	135	150	180	200
TX power (dBm)										
RX sensitivity (dB)										
RX sensitivity (dB)										

5GHZ 802.11AC 80 MHZ, WCN RADIO

	MCS0	MCS1	MCS2	MCS3	MCS4	MCS5	MCS6	MCS7	MCS8	MCS9
Data rate (Mbps)	32.5	65	97.5	130	195	260	292.5	325	390	433.3
TX power (dBm)										
RX sensitivity (dB)										

NOTE: 1. Receiver sensitivity and Transmitter Power tolerance is +-2dB.

7. Module mechanical characteristics

FIGURE 7-1. TOBUFI WITH INTERPOSER MECHANICAL DRAWINGS

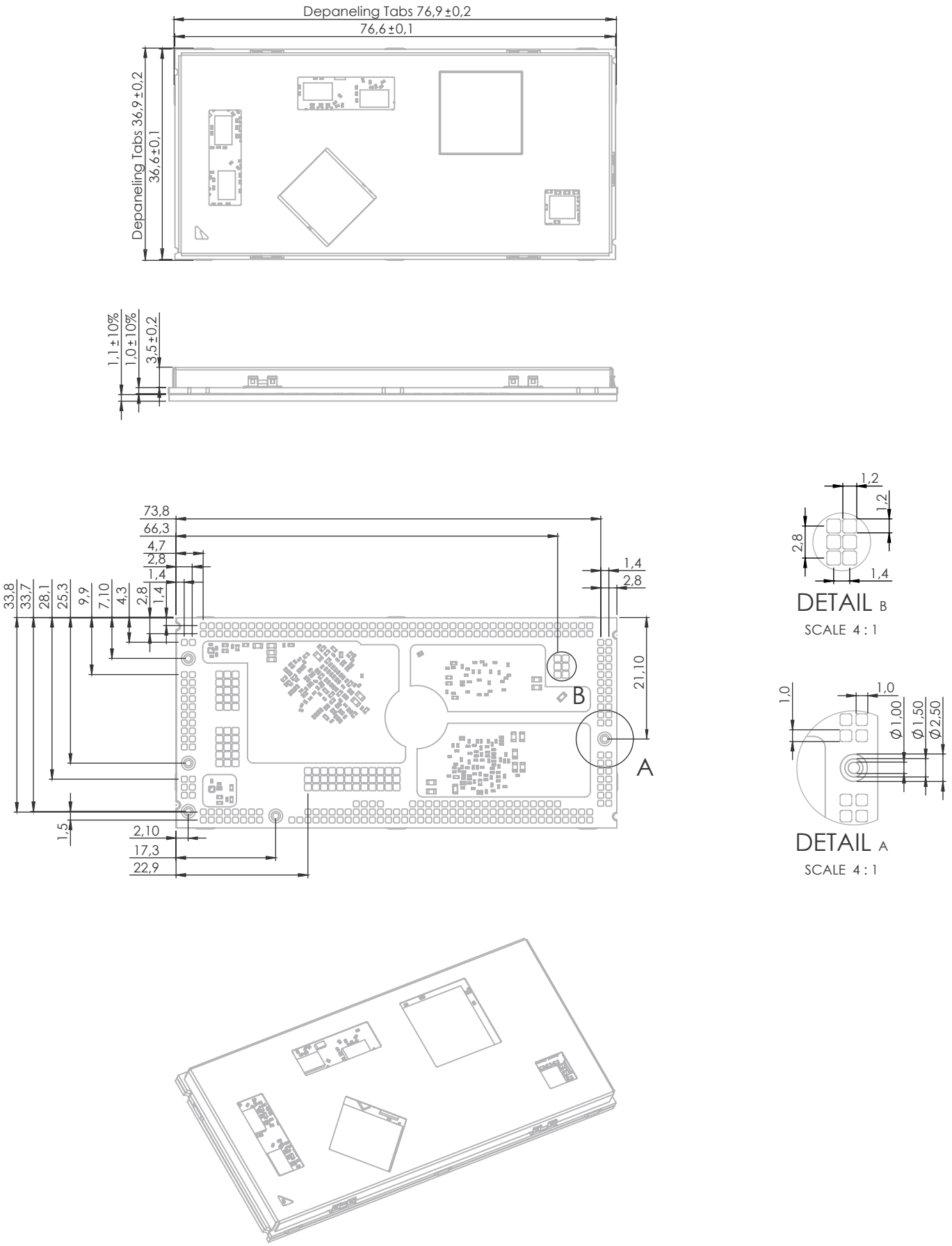
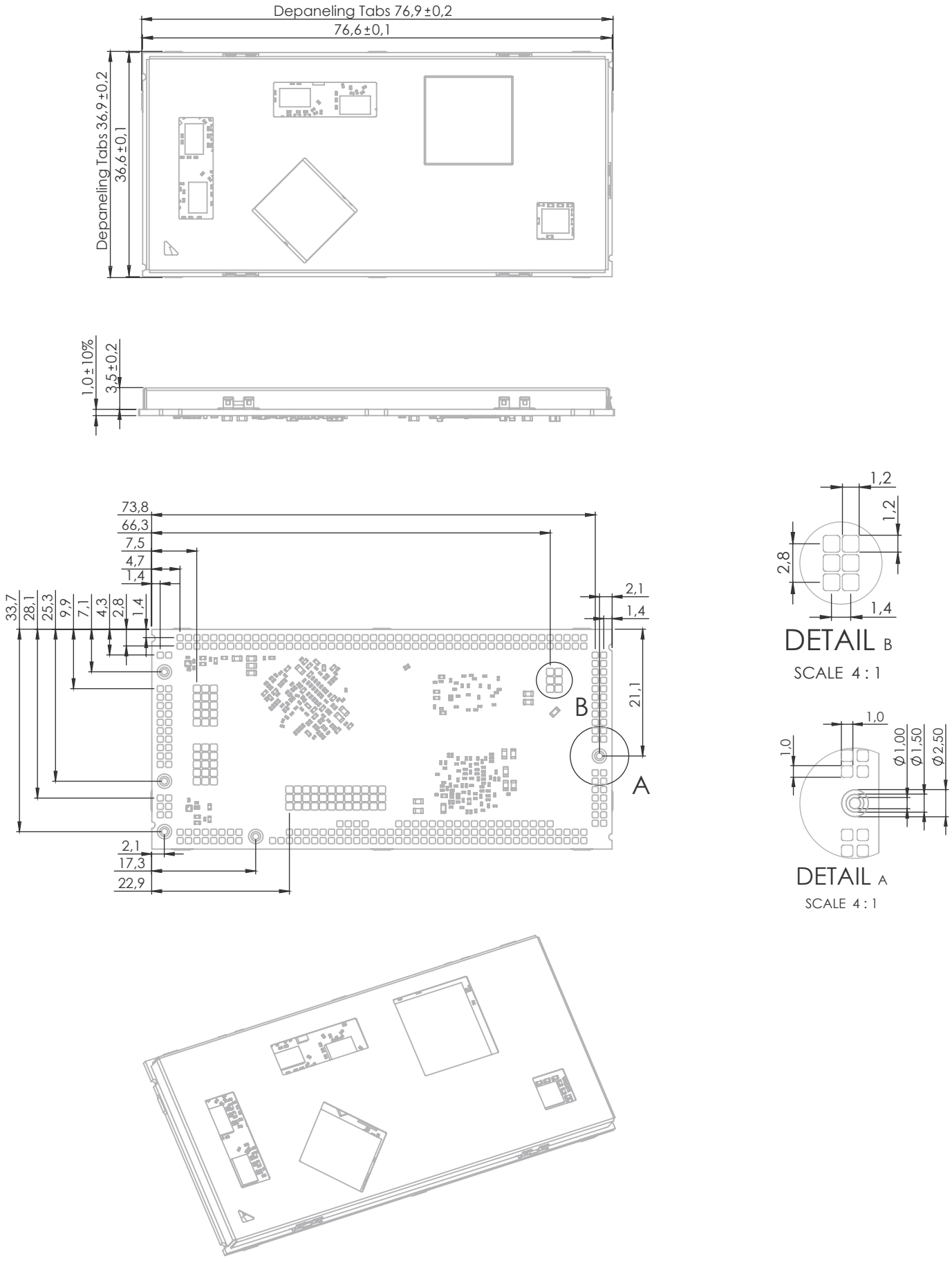


FIGURE 7-2. TOBUFI-NI WITH NO INTERPOSER MECHANICAL DRAWINGS



NOTE: The interposer is an additional PCB that serves as a standoff layer, allowing the TobuFi module to be mounted on a completely flat surface. Without the interposer, holes must be cut into the host PCB to accommodate the module.

8. Reflow profile recommendations

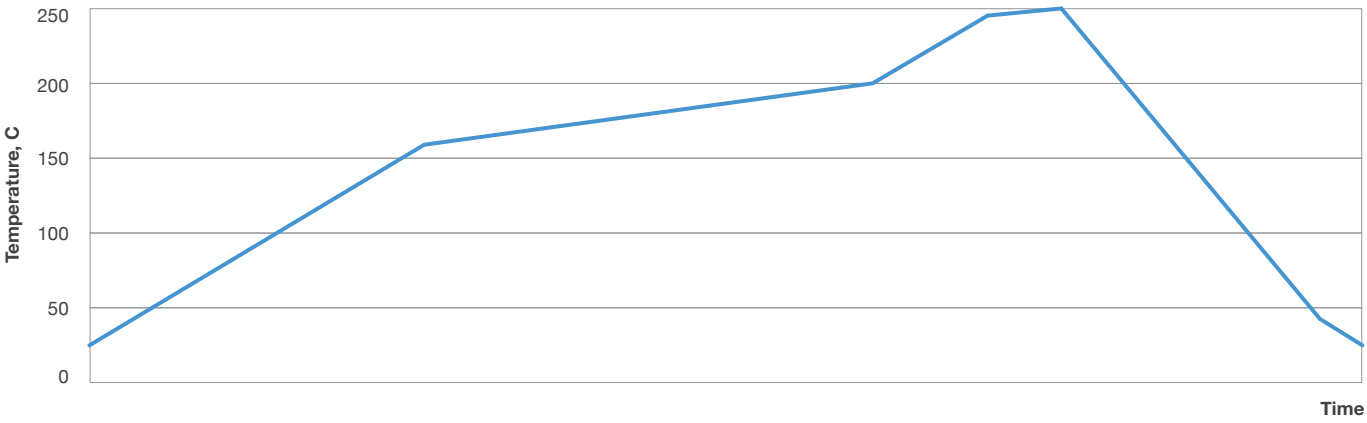
8.1. REFLOW PROFILE RECOMMENDATION

Reflow profile recommendation			
Pre-heat	**Min pre-heat temperature**	^{0}C	150
	Max pre-heat temperature	^{0}C	200
	Pre-heat time	s	150
	Ramp up rate	^{0}C/s	3
Ramp down rate	**Maximum time maintained above 220**	s	120
	Peak temperature	^{0}C	250
	Maximum time within 5^{0}C of peak temperature	s	30
Cooling	**Ramp down rate**	^{0}C/s	4

For optimal soldering of the Tobufi module, a stencil thickness of ≥100 µm is recommended. Solder paste aperture areas should be reduced by approximately 40% relative to the pad size to control paste volume.

NOTE: The Tobufi module is supplied with reflow ready solid solder plating on the pads. The stencil and paste recommendations above are provided to ensure consistent and reliable solder joint formation during the reflow process when mounting the module to the PCB.

8.2. REFLOW PROFILE



9. Design Guidelines

9.1 USB 2.0 PORT

Cover the USB 2.0 differential data lines with a continuous solid ground plane without breaks in the plane. Do not route the USB data lines underneath components or across other signal traces.

Trace Impedance	90 Ω ±15% differential
Intrapair length matching	<2mm
Recommended total routing length	<170mm
Polarity reversal	SSTX and/ or SSRX lines
Recommended spacing: SSTX to SSRX lane	> 3× line width
Recommended spacing: differential pairs to other signals	> 4× line width

9.2 USB 3.0 PORT

Cover the USB 3.0 differential data lines with a continuous solid ground plane without breaks in the plane.
Do not route the USB data lines underneath components or across other signal traces.

- The differential pair leading into SSRX at the module requires 0.1 µF AC coupling capacitors. These should be placed as close as possible to the transmitter or connector to ensure proper operation.
- The module provides AC coupling capacitors for SSTX lines; external capacitors for these lines are not recommended.
- The package size of the required capacitors must not exceed 0402.

Trace Impedance	90 Ω ±15% differential
Intrapair length matching	<0.127mm
Interpair length matching	<3.81mm
Recommended total routing length	<170mm
Polarity reversal	SSTX and/ or SSRX lines
Recommended spacing: SSTX to SSRX lane	>3× line width
Recommended spacing: differential pairs to other signals	>4× line width

9.3 HDMI

Route HDMI differential pairs with continuous controlled impedance and without discontinuities. Ensure minimal impedance variation along the entire path. Right angle bends on HDMI traces must be avoided.
To protect against ESD events:

- Place 5 V working voltage TVS diodes close to the HDMI connector on non differential lines.
- Low capacitance TVS diodes can also be used on differential pairs
- TVS diodes should be placed as close to the HDMI connector as possible.

Trace Impedance	100 Ω ±15% differential
Polarity reversal	Not allowed
Intrapair length matching	<0.7mm
Interpair length matching	<3mm
Recommended spacing: TDMS to other signals	>4× line width
Recommended spacing: TDMS to TDMS	>3× line width
Recommended spacing: differential pairs to other signals	>4× line width

9.4 SDC

SDC signal lines must be isolated from noise sources above, below, and adjacent to the routing layer.

Nominal trace impedance	36-50 Ω
Recommended total routing length	<75mm
SDC CLK to DATA and CMD length matching	<6mm

9.5 RGMII

The following layout requirements apply for the RGMII interface:

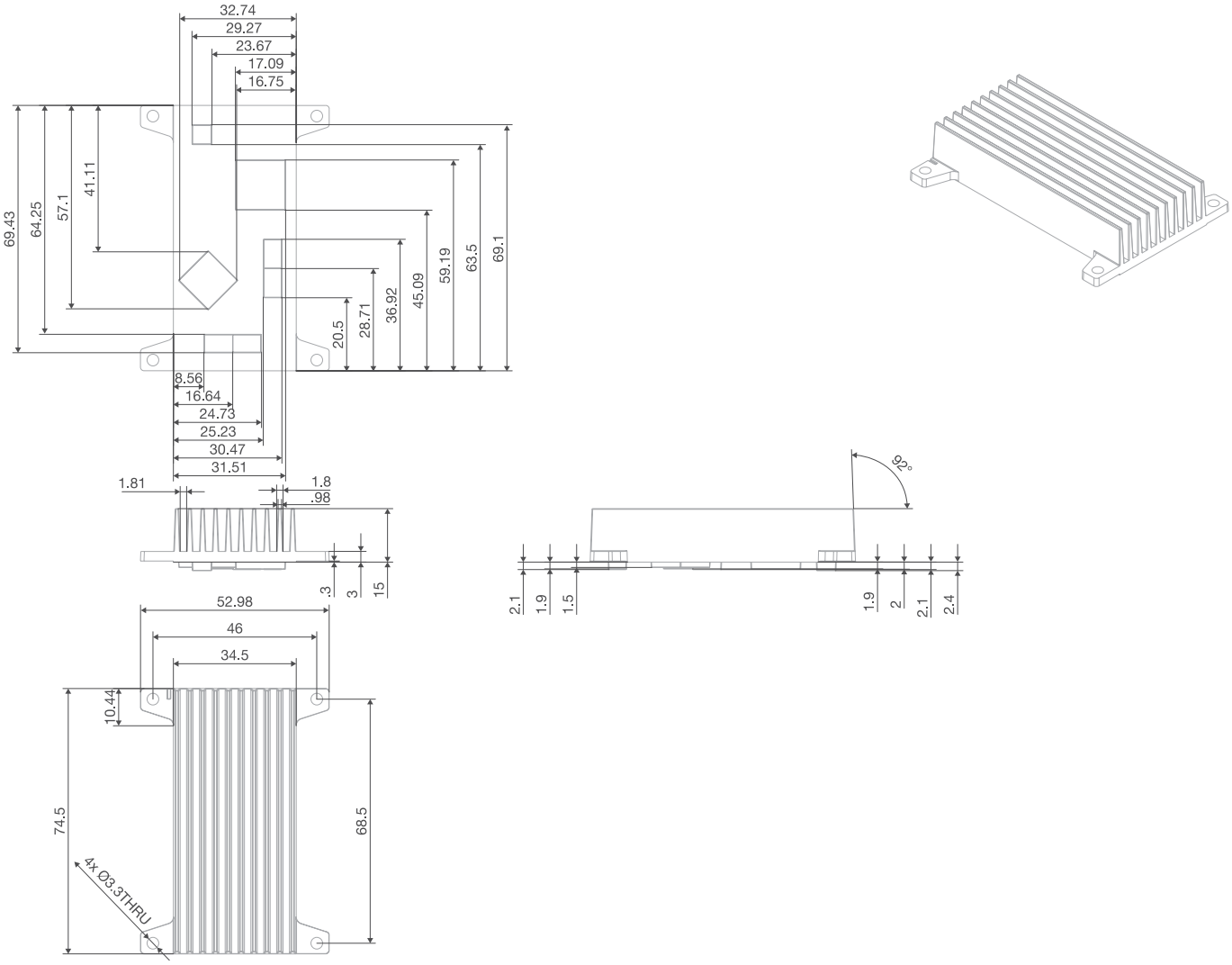
Nominal trace impedance	50 Ω ±20%
Maximum trace length	180mm
Recommended length matching for TX-CLK to TX-CTL, TX-DATA to TX-DATA	<10mm
Recommended length matching for RX-CLK to RX-CTL, RX-DATA to RX-DATA	<10mm
Recommended spacing: within Tx (CLK to DATA/CTL) bus or Rx bus (CLK to DATA/CTL)	>2× line width
Recommended spacing: Tx bus to Rx bus	>2× line width
Recommended Spacing to all other signal	>3× line width

9.6 PCB LAYOUT GUIDELINES

To ensure optimal performance it is important to follow schematic and layout references carefully.
A PCB with a minimum of four layers, with inner layers containing continuous ground copper pour, is recommended to ensure optimal signal integrity. Ground copper pour should be kept as uniform and uninterrupted as possible, particularly beneath high speed and antenna traces.
The supply voltage should be decoupled as close as possible to the VDD pads using X7R capacitors. Refer to the reference schematics for recommended decoupling capacitor values.
The module's antenna outputs are designed for use with a 50 Ω single ended antenna. An antenna matching circuit consisting of three 0402 components is recommended between the module and antenna to allow impedance matching for a given antenna in the PCB design, ensuring optimum RF load impedance. Antenna traces should be kept as short as possible with minimal bends.
Antenna traces must be routed with a controlled impedance of 50 Ω. Avoid routing antenna traces over PCB layer changes to prevent signal reflections and/or RF output attenuation.
Long power supply traces on the PCB should be avoided. Each module ground pad should connect through at least one via to an inner ground plane.
Fast switching digital signals should not be routed close to the power supply or antenna traces.

10. Thermal considerations, heatsink

TobuFi DVK is sold with heatsink, which surface area is 214cm2 and made from aluminum. It is recommended to keep the same surface area for the TobuFi module.



11. Laminate Conditions

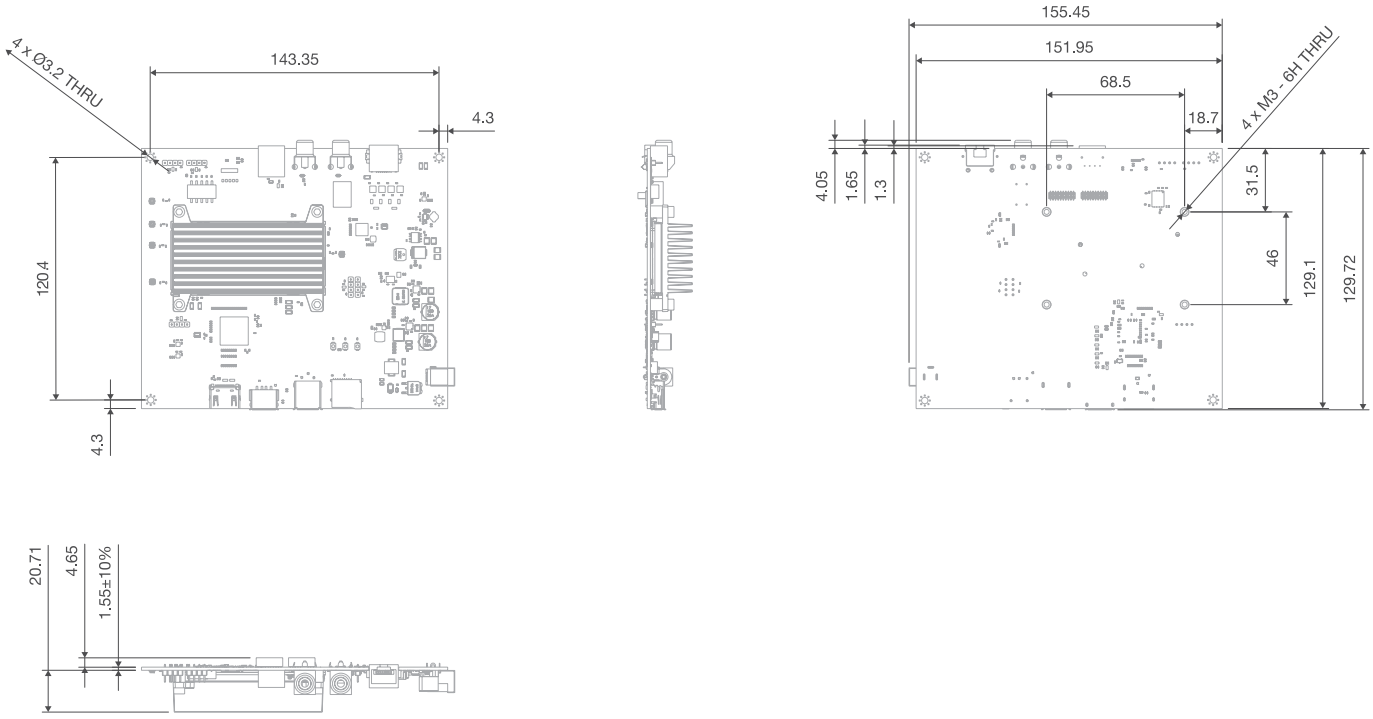
8devices modules are manufactured according to the standard IPC-A-610 Norm Class 2. Standard states: “Bow/twist after solder should not exceed 1.5% for through-hole and 0.75% for surface mount printed board applications”. According to this statement, TobuFi module can be bowed and twisted up to 0.577mm. To avoid negative effects of bow and twist we recommend to increase the paste thickness for the module pads to achieve better co-planarity.

FIGURE 11-1. EXAMPLE OF BOW AND TWIST

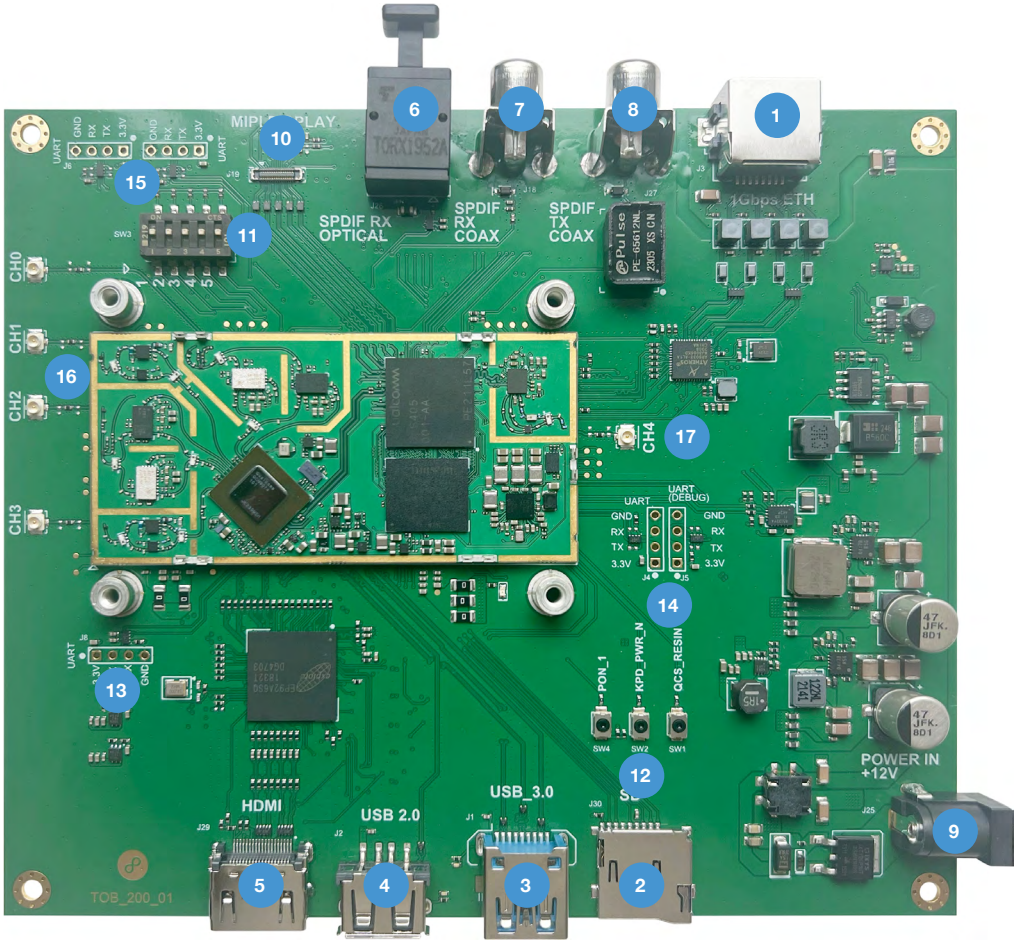
Bow **Twist**

12. Development board

12.1. DVK DIMENSIONS

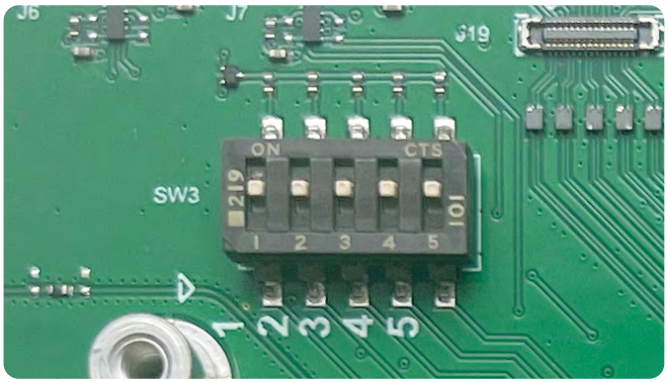


12.2. DVK INTERFACES



1. 1Gbps Ethernet
2. SD card slot
3. USB 3.0 interface
4. USB 2.0 interface
5. HDMI connector
6. Spdif RX optical
7. Spdif RX coax
8. Spdif TX coax
9. 12V Power supply
10. Connector for MIPI display
11. Configuration switch
12. Buttons
13. QCN UART
14. Debug UART and additional UART
15. Two additional UARTs
16. QCN RF ports
17. WCN RF port

12.3. BOOTSTRAP SWITCH



Boot Config	1	2	3	4	5
eMMC -> SD -> USB 2.0	OFF	OFF	OFF	OFF	OFF
SD -> eMMC -> EDL	OFF	OFF	OFF	OFF	ON
eMMC -> EDL	OFF	OFF	OFF	ON	OFF
USB 2.0	OFF	OFF	OFF	ON	ON
Parallel NAND (No NAND)	OFF	OFF	ON	OFF	OFF
NOR Flash -> EDL	OFF	OFF	ON	OFF	ON

13. TobuFi packaging and ordering info

TobuFi modules are packed into trays. Each tray fits 16 modules. Every 5 trays are vacuum sealed and one standard packaging box contains 400 modules.

FIGURE 13-1. TOBUFI TRAY DIMENSIONS

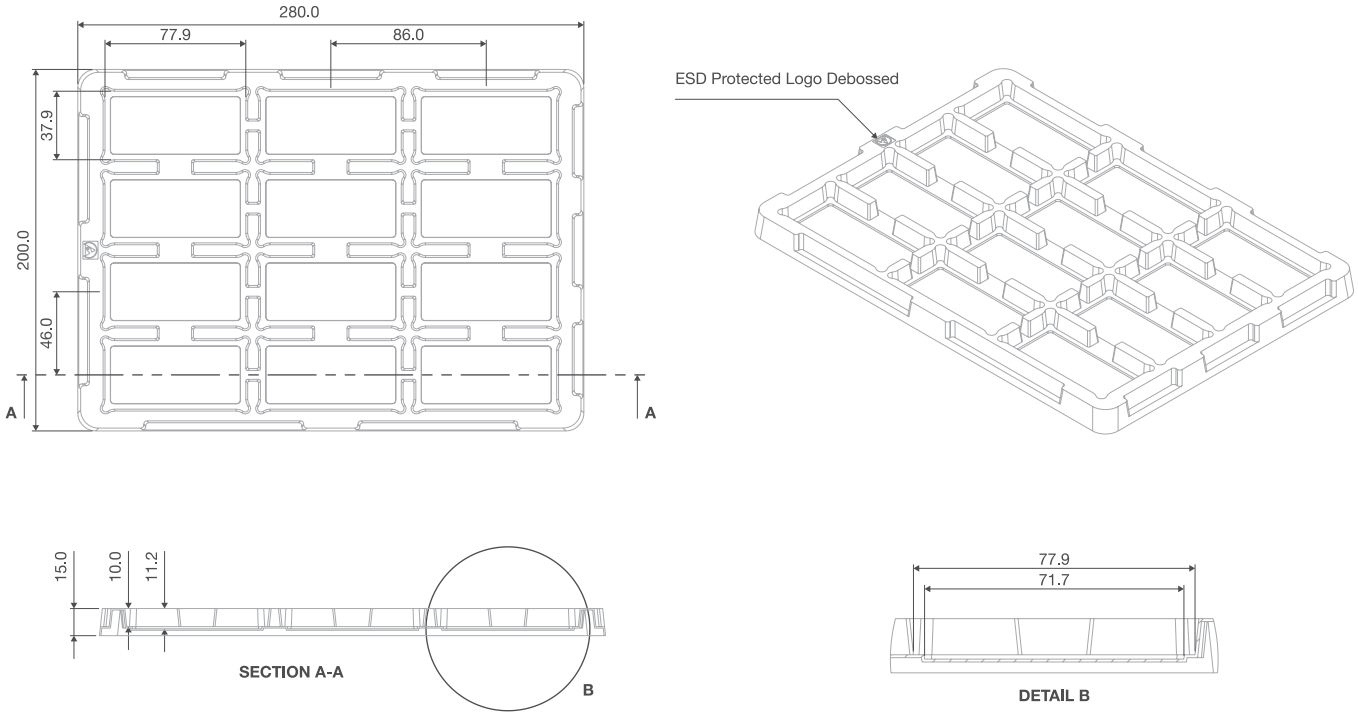


FIGURE 13-2. STANDARD PACKAGING BOX DIMENSIONS

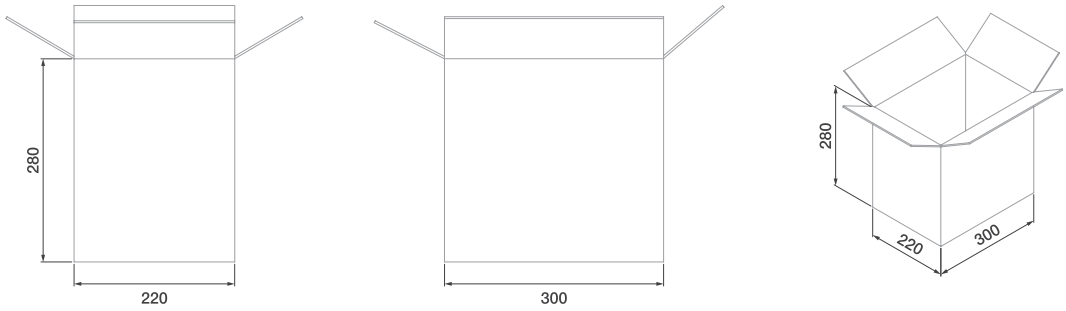


TABLE 13-1. ORDERING PART NUMBERS

Order Number	Description
TobuFi	TobuFi module, Radio 1: 2.4GHz+5GHz, with interposer,industrial temperature range -40°C to 85°C
TobuFi26	TobuFi module, Radio 1: 2.4GHz+6GHz, with interposer,industrial temperature range -40°C to 85°C
TobuFi-NI	TobuFi module, Radio 1: 2.4GHz+5GHz, no interposer,industrial temperature range -40°C to 85°C
TobuFi26-NI	TobuFi module, Radio 1: 2.4GHz+6GHz, no interposer,industrial temperature range -40°C to 85°C
TobuFi-DVK	Development kit, based on TobuFi-NI module
TOB_100_M03_02	Aluminum heatsink radiator for TobuFi module

14. Document Revision History

Revision	Revision Date	Description
v1.0	2023-10-09	Initial release
v1.1	2024-07-01	Updated Pinout diagram
v1.2	2025-01-20	Updated quick specs with new option information, added mechanical drawings for NI version, added new order numbers
v1.3	2025-08-18	Updated quick specs, TABLE 1-1 (WIFI), FIGURE 3-1, TABLE 3-1, TABLE 3-2, TABLE 3-4, TABLE 3-5, TABLE 3-6, TABLE 3-7, TABLE 3-8, TABLE 3-10, TABLE 3-11, TABLE 3-12, TABLE 3-16, FIGURE 7-1, FIGURE 7-2, Added stencil thickness and paste recommendations, added design guidelines
v1.4	2025-09-04	Updated FIGURE 7-1, FIGURE 7-2, TABLE 13-1, added a note about interposer purpose