PAT9102DM-T4QU: Optical Tracking Chip

General Description

The PAT9102 is PixArt Imaging's high performance Optical Tracking Chip (OTC), using low power CMOS chip designed specifically for dual axis tracking on surfaces in printer and automation applications. The OTC offers high accuracy with repeated error of 0.15 % over 25 mm of media movement with speeds up to 20 inches per second (ips). The OTC integrates light source and optical chip with built in picture element recognition engine and DSP that provides the host system real-time feedback.

Key Features

- Dual axis tracking chip
- Integrated 16 pins molded lead-frame DIP package
- High accuracy with repeated error of 0.15 % over 25 mm travel distance
- High resolution of 17904 cpi
- Supports Four-Wire Serial Port Interface (SPI)
- External interrupt output for motion detection
- Internal Oscillator – no clock input needed

Applications

- Print media applications
- Scanners
- Machine vision and automation

Key Parameters

Parameter	Value
Supply Voltage (V)	V_{DD}: 3.0 – 3.6 V_{DDIO}: 3.0 – 3.6
LED Supply Voltage (V)	V_{LED}: 3.0 – 3.6
Raw Data Array	32 Col x 32 Row
Interface	4-Wire SPI @ 2 MHz
Repeated Error (%)	0.15 (± 0.0375 mm over 25 mm travel distance)
Frame Rate (fps)	3600
Speed (ips)	20
Acceleration (m/s^2)	4
Resolution (cpi)	17904
Z Height (mm)	2.4
Optical Lens Magnification	1:1
Package Type	16 pin DIP package with LM19-LSI lens: 18.85 x 21.15 x 7.41 mm^3 16 pin DIP package with L0AE-LSI1 lens: 10.90 x 16.20 x 7.41 mm^3

Ordering Information

Part Number	Package Type
PAT9102DM-T4QU	16-pin DIP Package
LM19-LSI	Lens
L0AE-LSI1	Trim Lens

RoHS compliant

For any additional inquiries, please contact us at https://www.pixart.com

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1.0 Signal Description

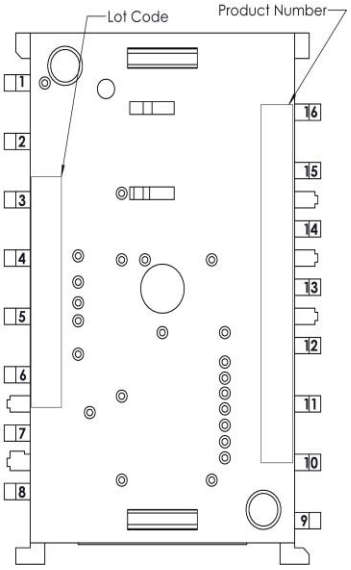


Figure 1. Pin Configuration

Table 1. PAT9102 Signal Pins Description

Pin No.	Signal Name	Type	Description
Power Supplies			
4	VDDA28	Power	Internal voltage output @ 2.8V
5	VDDA25	Power	Internal voltage output @ 2.5V
6	VDDD18	Power	Internal voltage output @ 1.8V
7	VDDIO	Power	I/O reference voltage
15	VDD	Power	Input power supply
16	VLED	Power	Supply to LED anode
1	LED_GND	Ground	LED Ground
2	AGND	Ground	Analog ground
8	DGND	Ground	Digital ground
Control Interface			
9	NCS	Input	Chip select
10	MOSI	Input	Serial data input
11	MISO	Output	Serial data output
12	SCLK	Input	Serial data clock
Functional I/O			
13	NRST	Input	Hardware reset
14	MOTION	Output	Motion interrupt
Data Interface			
3	NC	NC	No connection (float)

2.0 Operating Specification

2.1 Absolute Maximum Rating

Table 2. Absolute Maximum Rating

Parameter	Symbol	Min.	Max.	Unit	Note
Storage Temperature	T_S	-40	85	°C	
Supply Voltage	V_{DD}	-0.5	3.7	V	
	V_{DDIO}	-0.5	3.7	V	
	V_{LED}	-0.5	3.7	V	
Input Voltage	V_{IN}	-0.5	V_{DDIO} + 0.5	V	All I/O pins
ESD	ESD_{HBM}		2	kV	All pins (Human Body Model)

Notes:

1. Maximum Ratings are those values beyond which damage to the device may occur.
2. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum-rated conditions is not implied.
3. Functional operation should be restricted to the Recommended Operating Conditions.

2.2 Recommended Operating Condition

Table 3. Recommended Operating Condition

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Operating Temperature	T_A	0		40	°C	
Power Supply Voltage	V_{DD}	3.0	3.3	3.6	V	Including supply noise
	V_{DDIO}	3.0	3.3	3.6	V	Including supply noise
	V_{LED}	3.0	3.3	3.6	V	Including supply noise
Power Supply Noise				100	mV	Peak to peak. At the supply point to the chip
Serial Port Clock Frequency	f_{SCLK}			2	MHz	50% duty cycle
Distance from Lens Reference Plane to Tracking Surface	Z	2.10	2.40	2.70	mm	
Repeated Error	R		0.15		%	On white paper & photo paper at nominal height of 2.4mm @ 10 ips velocity over 25 mm travel distance @ 20 ips velocity over 50 mm travel distance
Frame Rate	F_R		3600		fps	
Speed	V			20	ips	Max constant velocity
Acceleration	A			4	m/s^2	Acceleration from stationary position
Resolution of motion report				17904	cpi	

Note: PixArt does not guarantee the performance of the system beyond the recommended operating condition limits.

2.3 DC Characteristics

Table 4. DC Electrical Specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply Current	I_{DD_RUN}		22		mA	Average current consumption, including LED[2] current with 1ms polling.
Power Down Current	I_{PD}		30		µA	
Input Low Voltage	V_{IL}			0.3 x V_{DDIO}	V	SCLK, MOSI, NCS
Input High Voltage	V_{IH}	0.7 x V_{DDIO}			V	SCLK, MOSI, NCS
Input Hysteresis	V_{I_HYS}		100		mV	SCLK, MOSI, NCS
Input Leakage Current	I_{LEAK}		± 1	± 10	µA	V_{in} = V_{DDIO} or 0V, SCLK, MOSI, NCS
Output Low Voltage	V_{OL}			0.45	V	I_{OUT} = 1mA, MISO, MOTION
Output High Voltage	V_{OH}	V_{DDIO} - 0.45			V	I_{OUT} = -1mA, MISO, MOTION

Notes:

1. All the parameters are tested under operating conditions: V_{DD} = 3.3V, V_{DDIO} = 3.3V, V_{LED} = 3.0V, Internal Clock = 80 MHz, Internal Slow Clock = 1 kHz, T_A = 25°C.
2. Typical pulse current drawn by V_{LED} is 55 mA.

2.4 AC Characteristics

Table 5. AC Electrical Specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Motion Delay After Navigation Start	$t_{MOT-NAV}$	35			ms	From navigation engine start to valid motion, assuming motion is present
Shutdown	t_{STDWN}			1.5	ms	From Shutdown mode active to low current
Wake from Shutdown	t_{WAKEUP}	5			ms	From Shutdown mode inactive to ready to accept IO command. Notes: A RESET must be asserted after a shutdown. Refer to Product Datasheet Section 5.2. Power-Down Sequence", also note $t_{MOT-NAV.}$
MISO Rise Time	t_{r-MISO}		50		ns	C_L = 100pF
MISO Fall Time	t_{f-MISO}		50		ns	C_L = 100pF
MISO Delay After SCLK	$t_{DLY-MISO}$			170	ns	From SCLK falling edge to MISO data valid, with 100pF load
MISO Hold Time	$t_{hold-MISO}$	200			ns	Data held until next falling SCLK edge
MOSI Hold Time	$t_{hold-MOSI}$	200			ns	Amount of time data is valid after SCLK rising edge
MOSI Setup Time	$t_{setup-MOSI}$	120			ns	From data valid to SCLK rising edge
SPI Time Between Write Commands	t_{SWW}	180			µs	From rising SCLK for last bit of the first data byte, to rising SCLK for last bit of the second data byte.
SPI Time Between Write And Read Commands	t_{SWR}	180			µs	From rising SCLK for last bit of the first data byte, to rising SCLK for last bit of the second address byte.
SPI Time Between Read And Subsequent Commands	t_{SRW} t_{SRR}	20			µs	From rising SCLK for last bit of the first data byte, to falling SCLK for the first bit of the address byte of the next command.
SPI Read Address-Data Delay	t_{SRAD}	160			µs	From rising SCLK for last bit of the address byte, to falling SCLK for first bit of data being read.
SPI Read Address-Data Delay for Burst Mode Motion Read	t_{SRAD_MOTBR}	35			µs	From rising SCLK for last bit of the address byte, to falling SCLK for first bit of data being read. Applicable for Burst Mode Motion Read only.
NCS Inactive After Motion Burst	t_{BEXIT}	500			ns	Minimum NCS inactive time after motion burst before next SPI usage

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
NCS To SCLK Active	$t_{NCS-SCLK}$	120			ns	From last NCS falling edge to first SCLK rising edge
SCLK To NCS Inactive (For Read Operation)	$t_{SCLK-NCS}$	120			ns	From last SCLK rising edge to NCS rising edge, for valid MISO data transfer
SCLK To NCS Inactive (For Write Operation)	$t_{SCLK-NCS}$	35			µs	From last SCLK rising edge to NCS rising edge, for valid MOSI data transfer
NCS To MISO High-Z	$t_{NCS-MISO}$			500	ns	From NCS rising edge to MISO high-Z state
MOTION Rise Time	$t_{r-MOTION}$		50		ns	C_L = 100pF
MOTION Fall Time	$t_{f-MOTION}$		50		ns	C_L = 100pF
Input Capacitance	C_{in}		50		pF	SCLK, MOSI, NCS
Load Capacitance	C_L			100	pF	MISO, MOTION
Transient Supply Current	I_{DDT}			33	mA	Max supply current during the supply ramp from 0V to VDD with min 150 µs and max 20 ms rise time. (Does not include charging currents for bypass capacitors)
	I_{DDTIO}			50	mA	Max supply current during the supply ramp from 0V to VDDIO with min 150 µs and max 20 ms rise time. (Does not include charging currents for bypass capacitors)

Note: All the parameters are tested under operating conditions: V_{DD} = 3.3V, V_{DDIO} = 3.3V, T_A = 25°C.

3.0 Mechanical Specifications

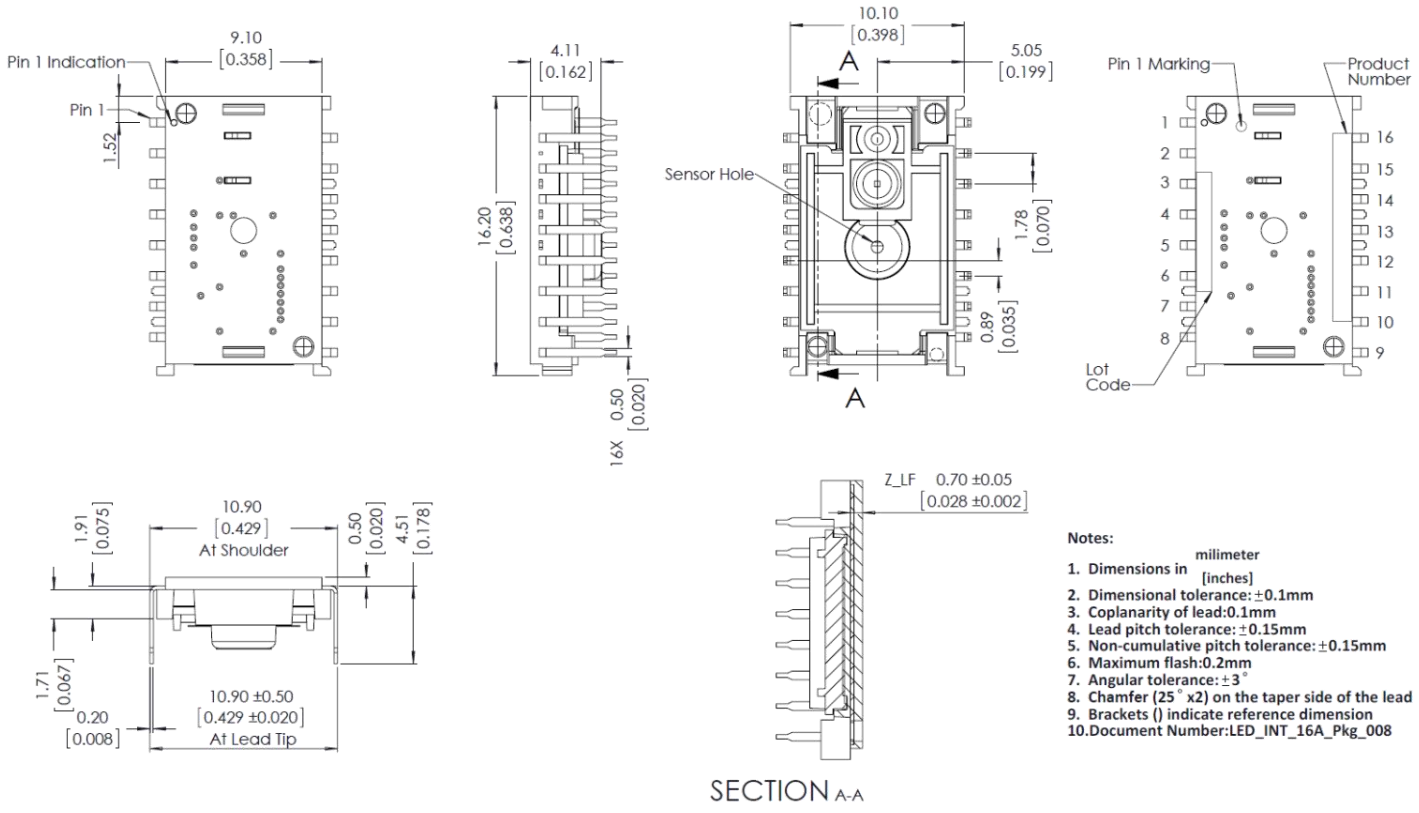
3.1 Package Marking

Refer to Figure 1. Pin Configuration for the code marking location on the device package.

Table 6. Code Identification

Code	Marking	Description
Product Number	PAT9102DM-T4QU	Chip part number label
Lot Code	AYWWXXXXXX	A: Assembly House Y: Year WW: Week XXXXXX: Reserved as PixArt reference

3.2 Package Outline Drawing



CAUTION: It is advised that normal static discharge precautions be taken in handling and assembling of this component to prevent damage and/or degradation which may be induced by ESD.

Figure 2. Package Outline Drawing

3.3 PCB Cutout

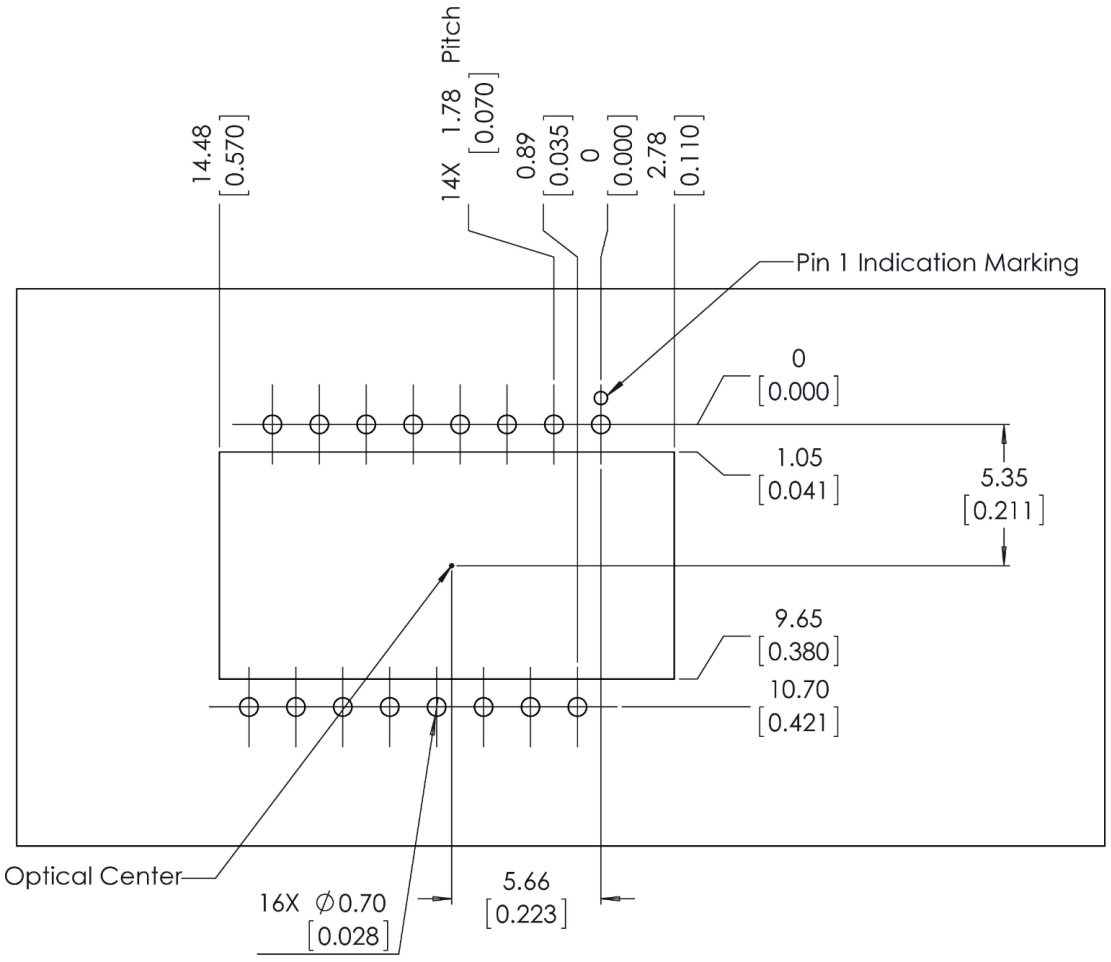


Figure 3. Recommended Chip Orientation, Mechanical Cutouts and Spacing (Top View)

3.4 LM19-LSI Lens Assembly Drawings

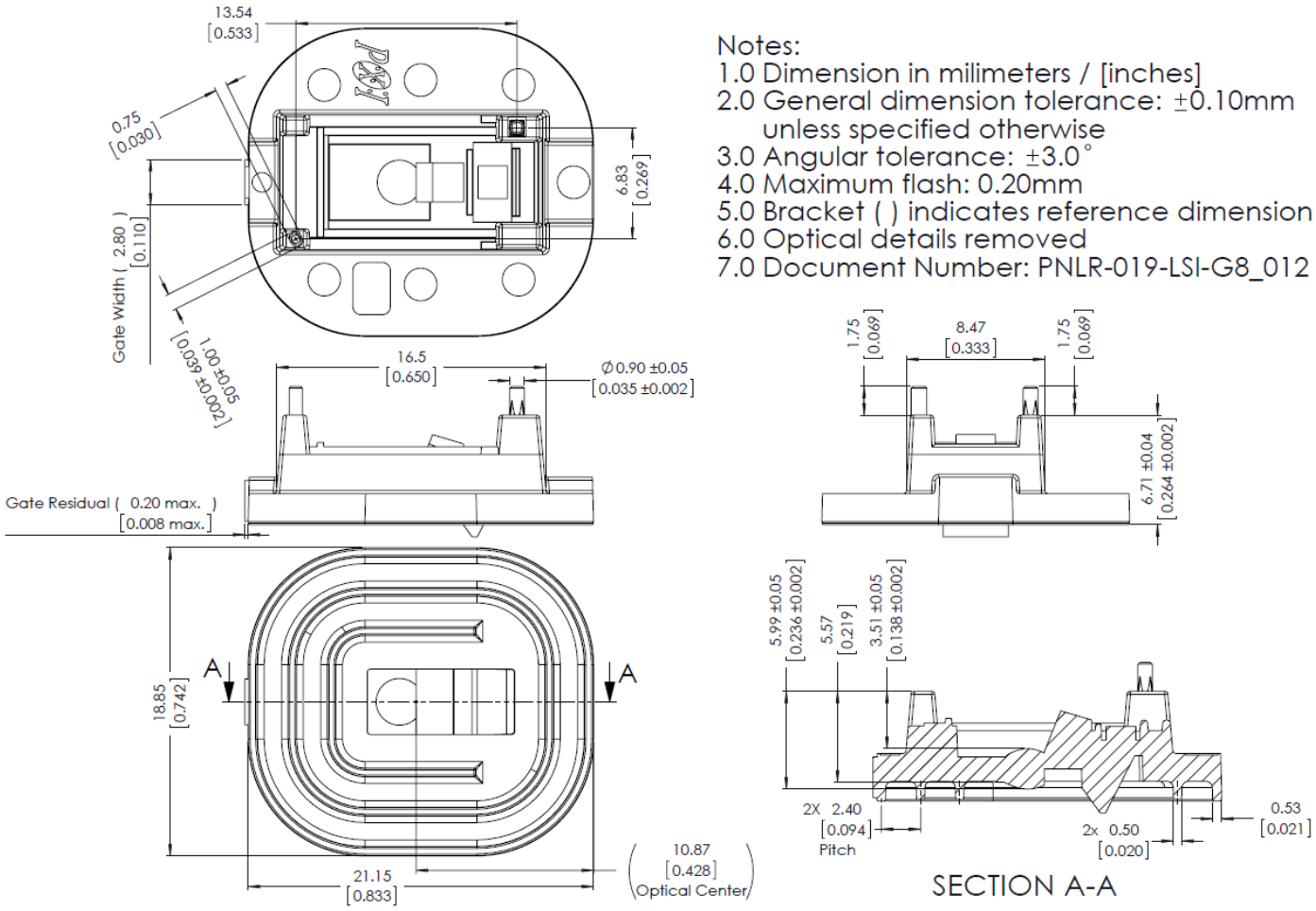


Figure 4. LM19-LSI Lens Outline Drawing

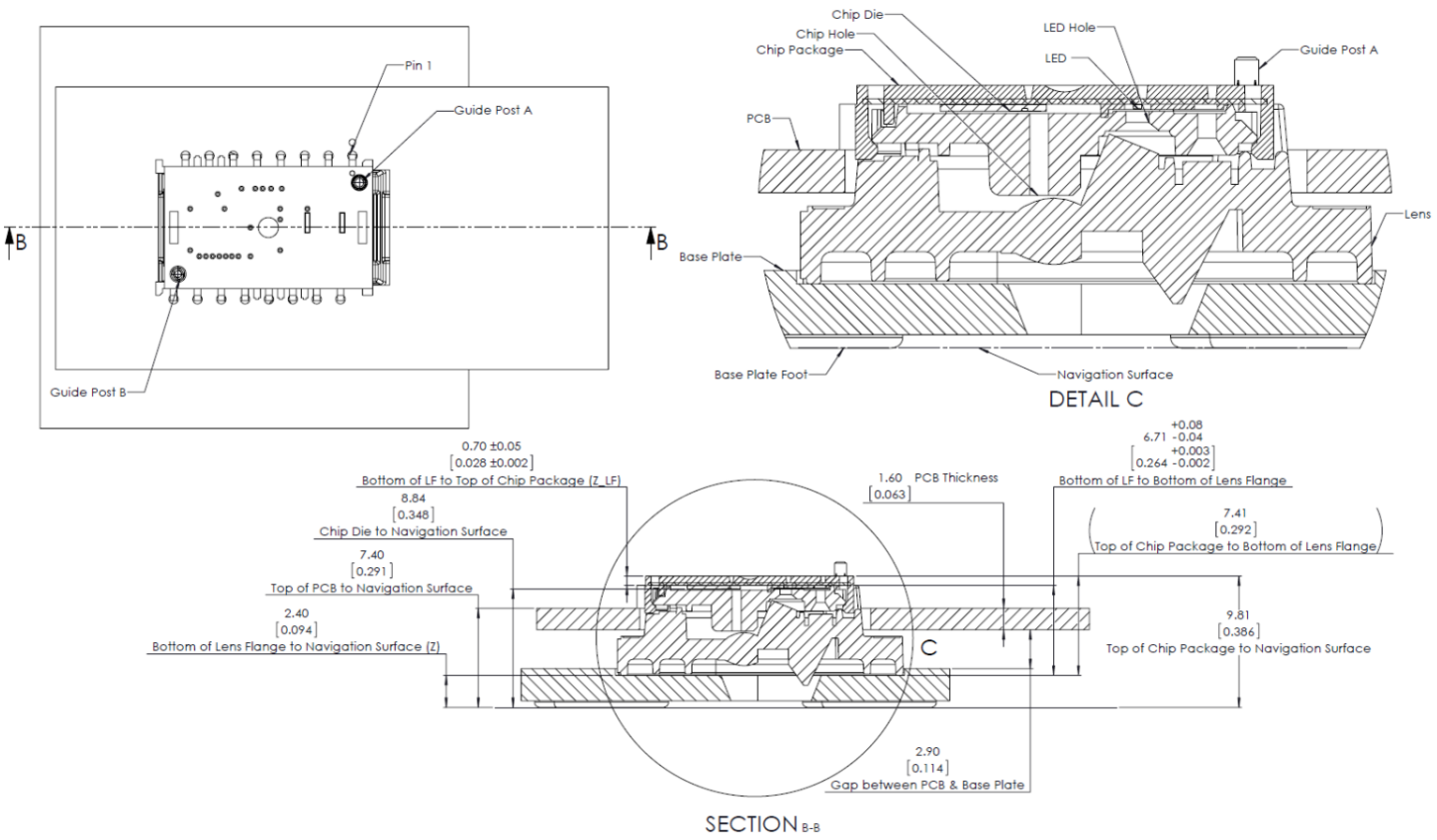


Figure 5. Assembly Drawing of PAT9102 and Distance from Lens Reference Plane to Tracking Surface (Z)

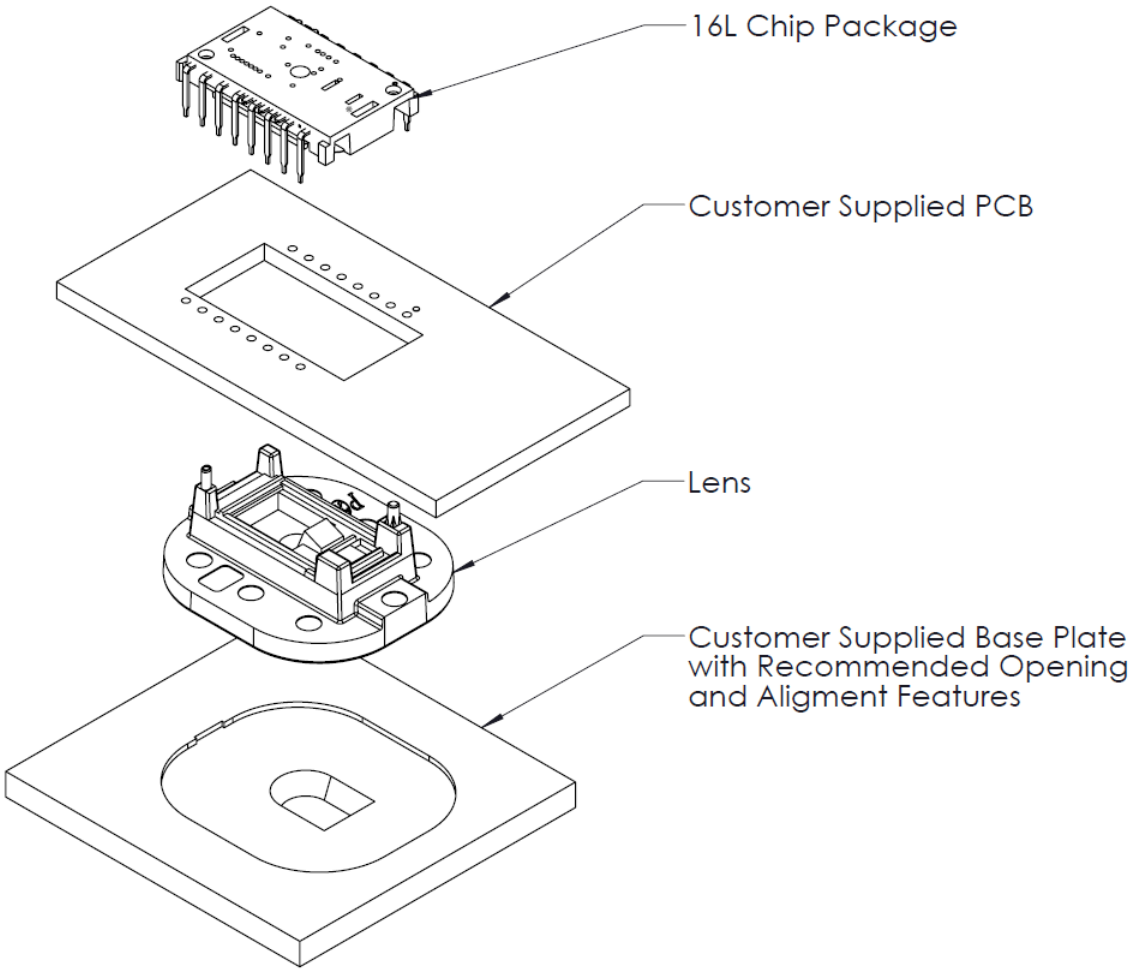


Figure 6. Exploded View of System Assembly with LM19-LSI Lens

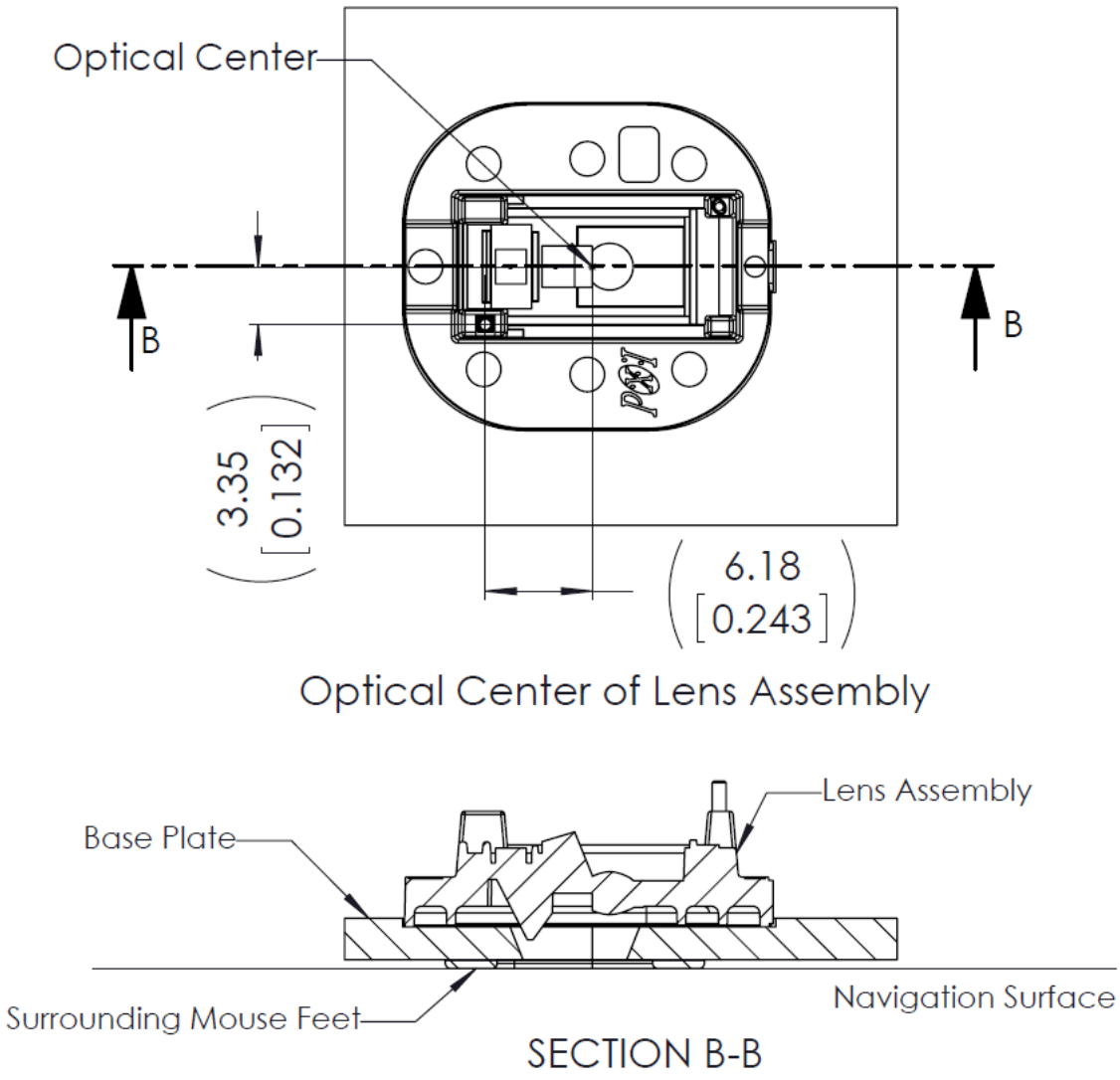


Figure 7. Cross Section View of LM19-LSI Lens Assembly

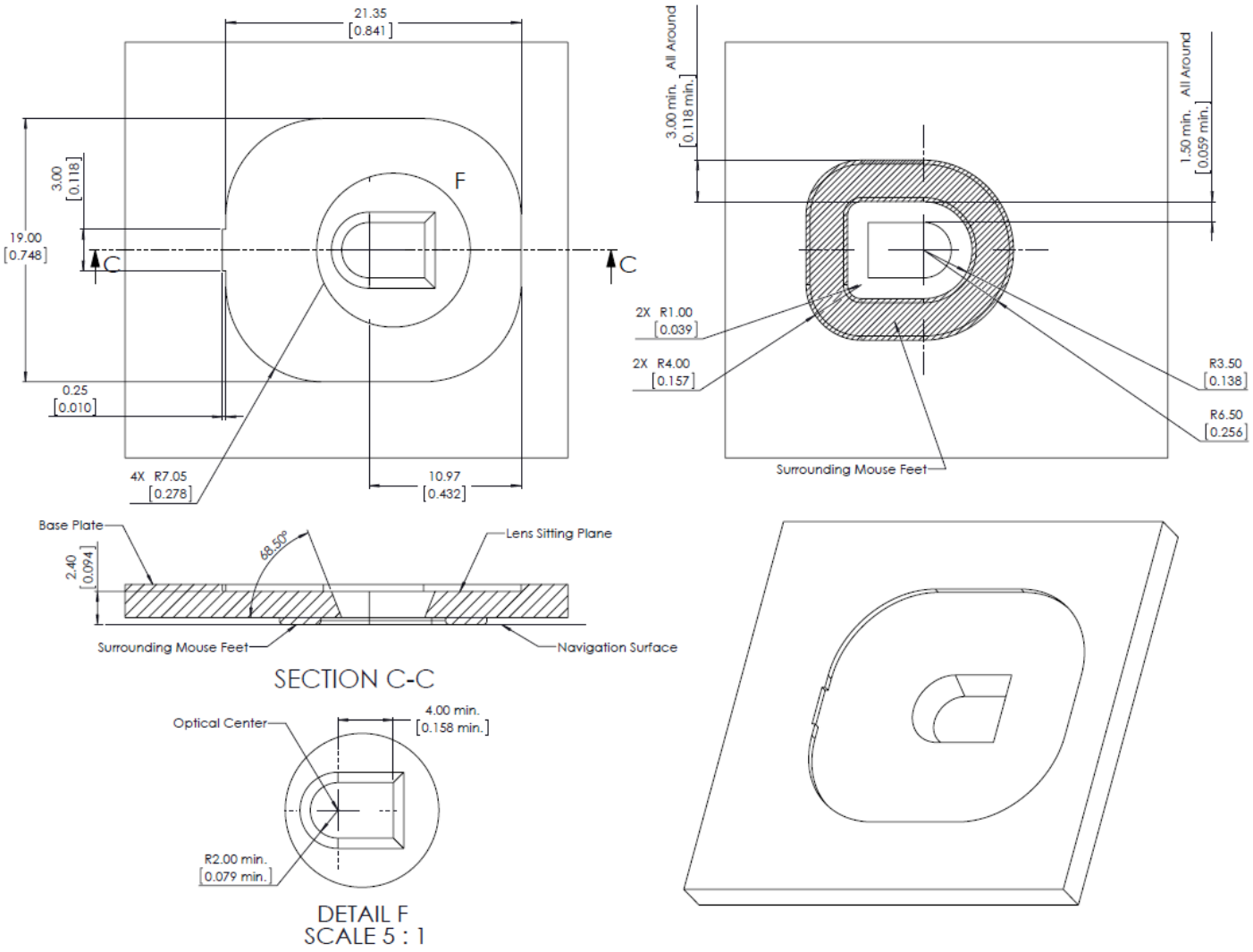


Figure 8. Recommended Base Plate Design with LM19-LSI Lens

3.5 L0AE-LSI1 Lens Assembly Drawings

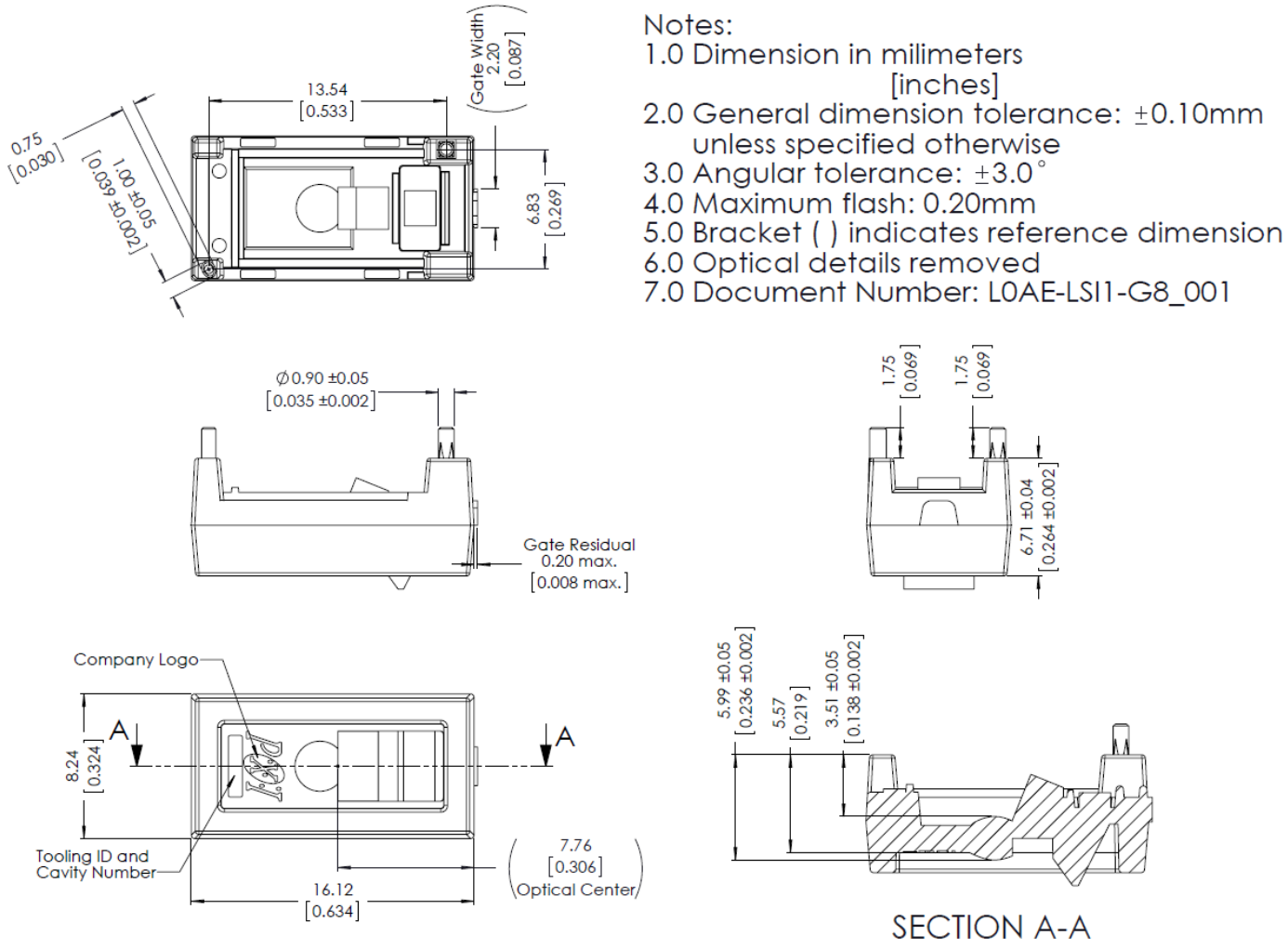


Figure 9. L0AE-LSI1 Lens Outline Drawing

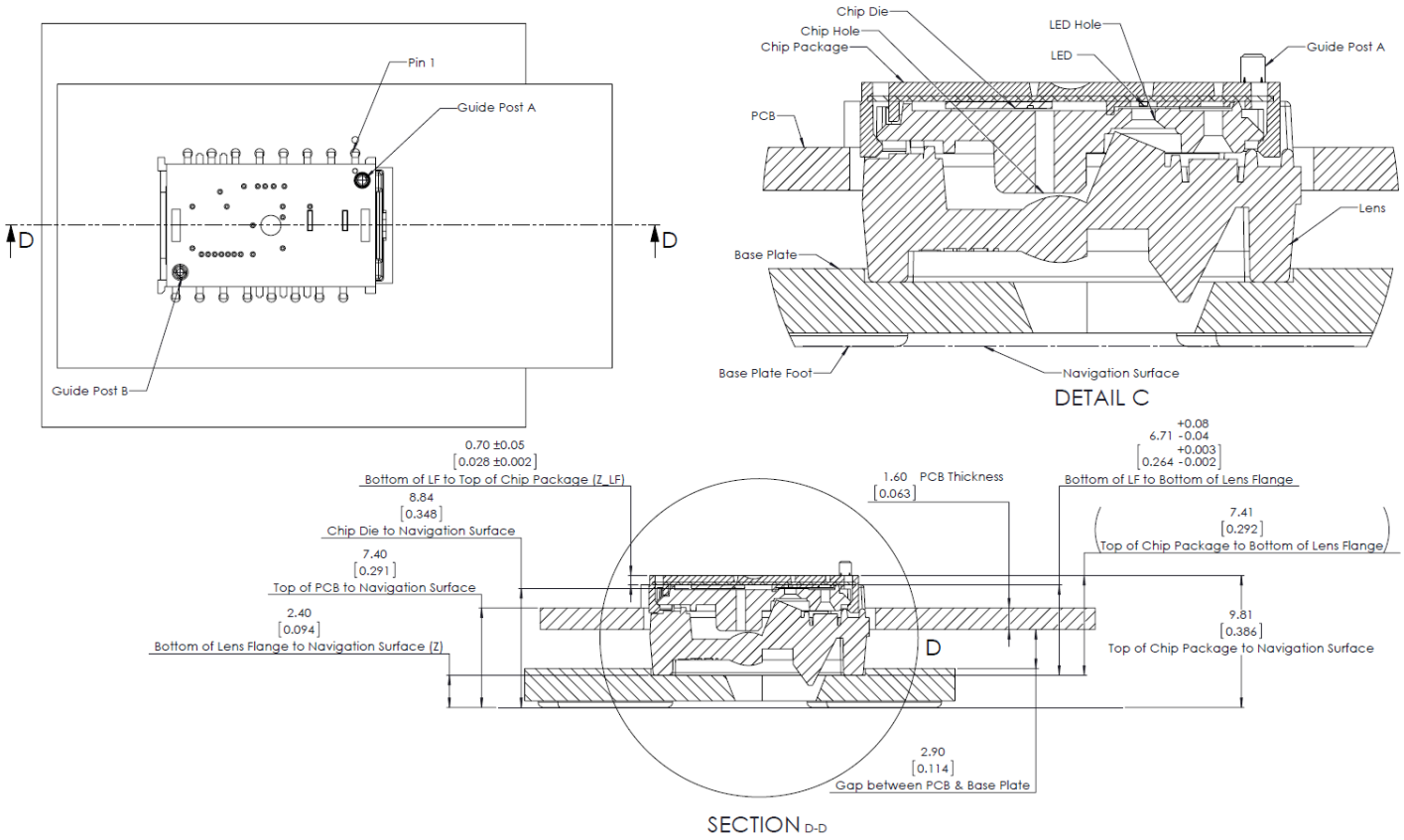


Figure 10. Assembly Drawing of PAT9102 and Distance from Lens Reference Plane to Tracking Surface (Z)

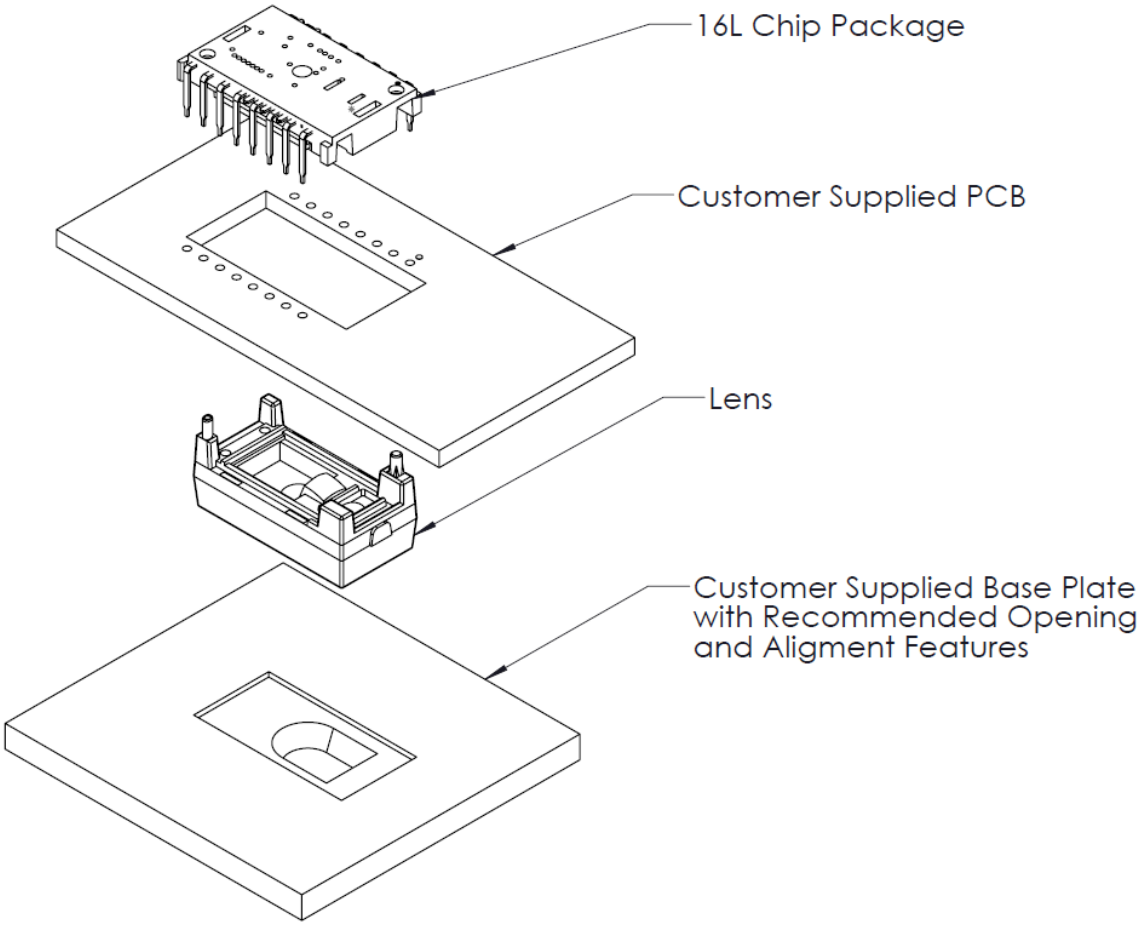


Figure 11. Exploded View of System Assembly with L0AE-LSI1 Lens

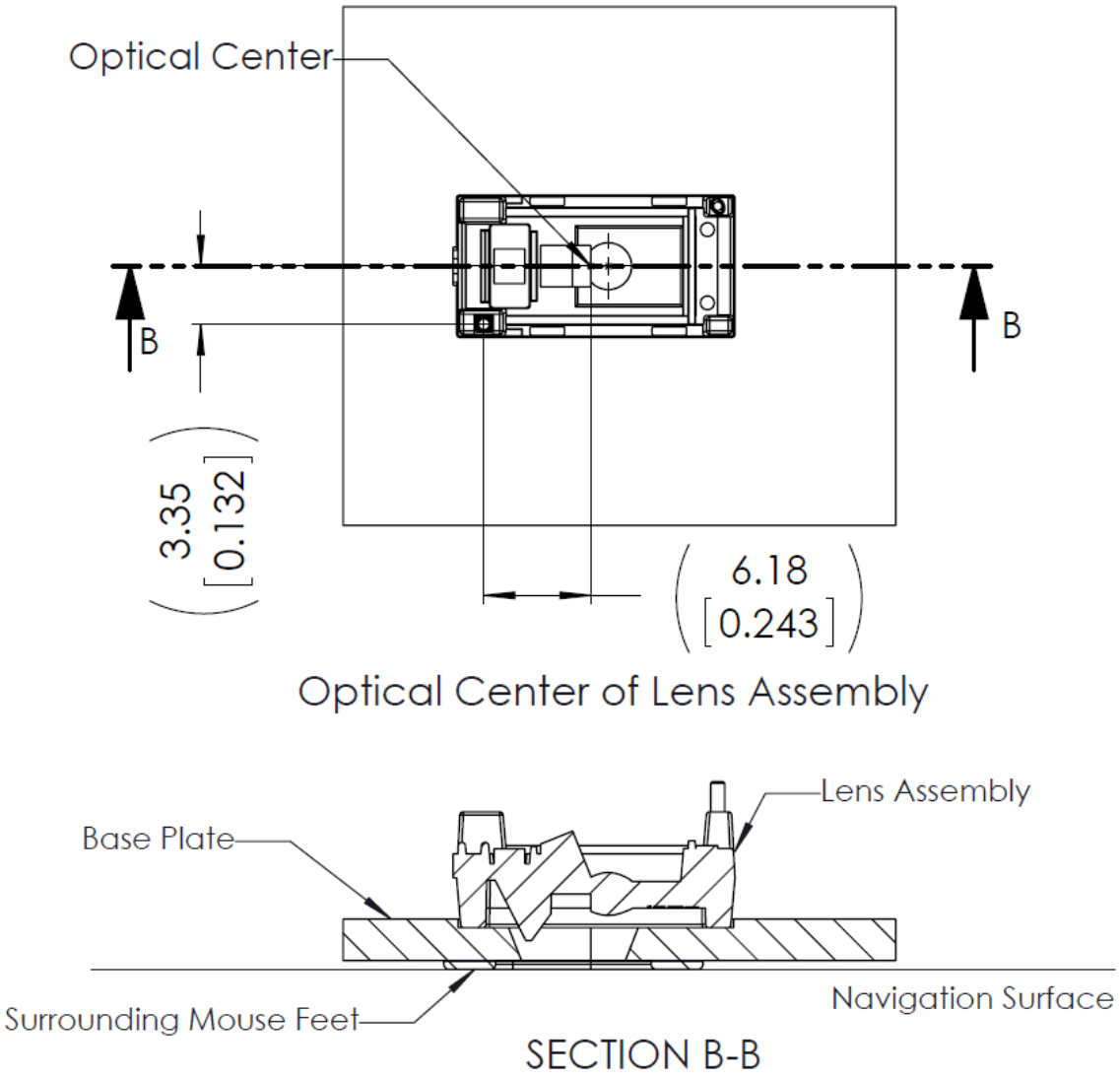


Figure 12. Cross Section View of L0AE-LSI1 Lens Assembly

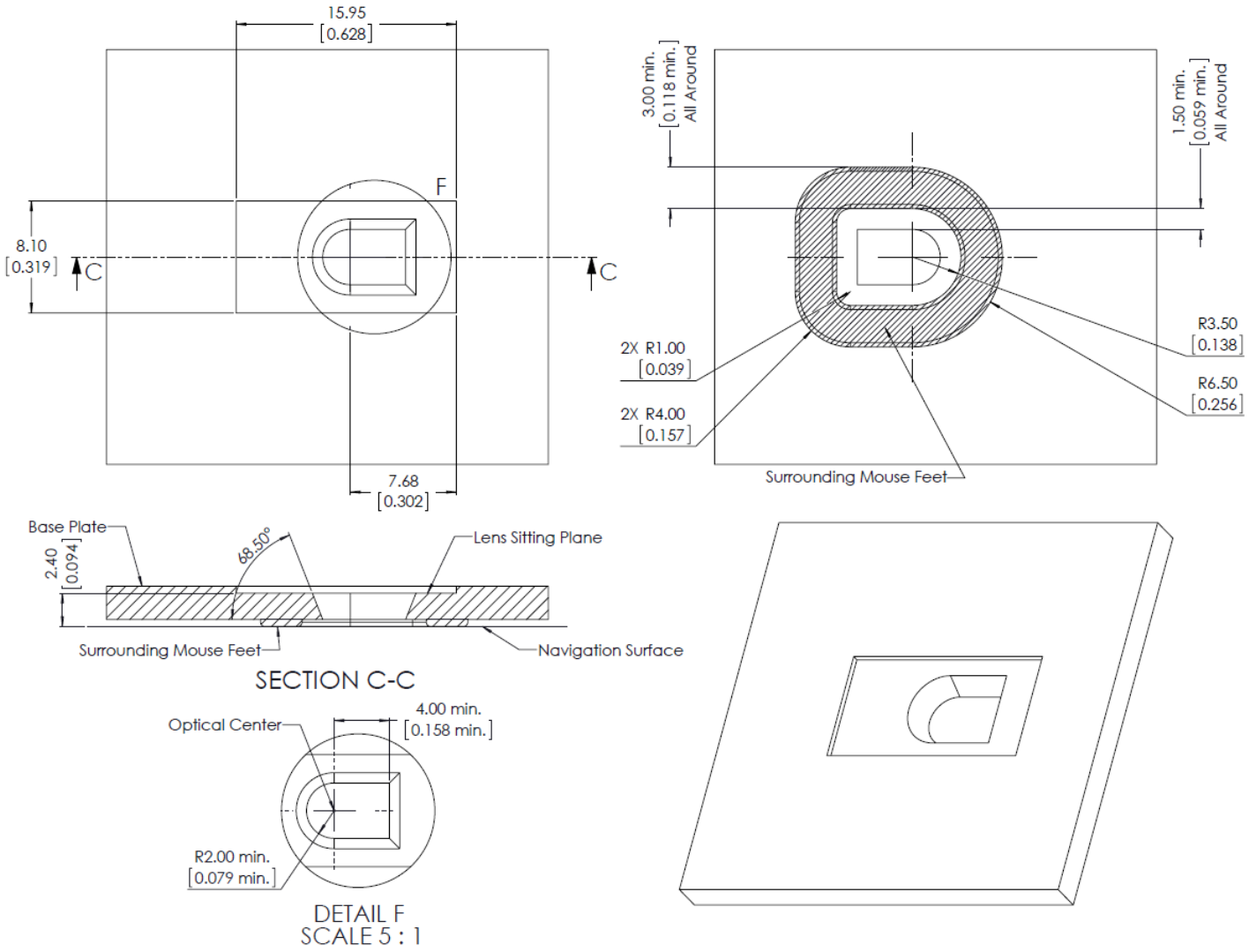
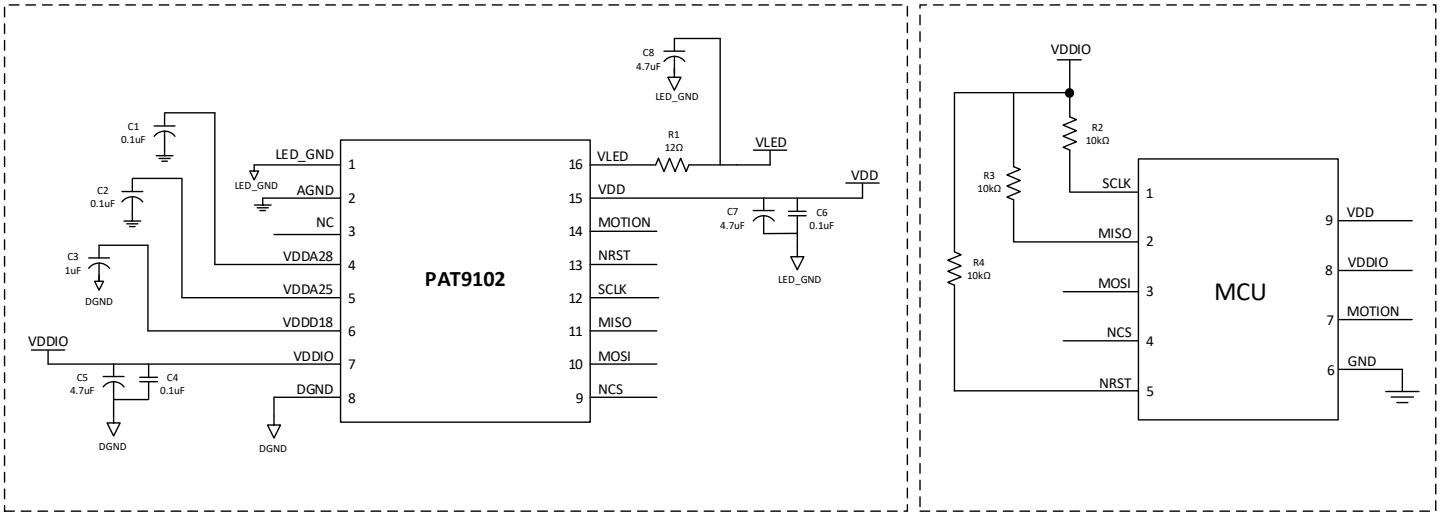


Figure 13. Recommended Base Plate Design with L0AE-LSI1 Lens

4.0 System Level Description

4.1 Reference Schematic



Note:
1. Capacitors must be placed near the chip.
2. LED's orientation is placed towards the palm of a hand.

External Component Type for PAT9102	Value	Quantity
Capacitor	0.1 µF	4
Capacitor	4.7 µF	3
Capacitor	1 µF	1
Resistor	12 Ω	1

Figure 14. PAT9102 Reference Schematics

Revision History

Revision Number	Date	Description
1.2	30 Apr 2019	Initial release
1.21	20 May 2021	Convert format