PAT9130EW-TKMT: Optical Tracking Miniature Chip

General Description

The PAT9130EW-TKMT is a high performance and high tracking speed optical tracking miniature chip using PixArt LASER-based optical navigation technology enabling surface tracking without an optical lens. It integrates an optical chip with a LASER light source in a single miniature package, providing wide depth of field (DOF) range, and design flexibility into highly space constraint devices. This tracking system also does not require a code wheel, a code strip and any special marking on the tracking surface for motion control or tracking purposes. Since the chip's tracking performance is susceptible to the contamination on the optical sensing area, it is recommended for use in hermetic or enclosed mechanical system design and applications.

Key Features

- Reflowable SMT package with built-in VCSEL LASER light source in a single package
- No lens is needed to work with the chip
- Wide DOF range on glossy metal surfaces
- High accuracy of tracking on glossy metal surfaces
- Tracking speed is up to 90 ips on glossy metal surfaces
- Support 3-wire SPI interface
- Programmable resolution up to 6,700 cpi with 50 counts/step
- Motion detection interrupt output
- Internal oscillator – no external clock input needed

Applications

- Devices that requires tracking on surfaces with wide DOF working range
- Devices that requires detecting the speed of fast moving surfaces
- Suitable for space-constraint devices

Key Parameters

Parameter	Value
Supply Voltage	VDD : 2.7 ~ 3.6V VDDA : 1.93V +/-0.05V (+/-2.5% voltage variation)
Control Interface	3-wire SPI
Max .Tracking Speed	Up to 90 ips on glossy metal surface Up to 35 ips on white copy paper
Max Resolution	Up to ~6,700 cpi
Operating current (@ VDD=3.3V and VDDA=1.9V)	Run : I_{VDD} = 0.5 mA, I_{VDDA} = 15 mA Power down : I_{VDD} = 2 µA, I_{VDDA} =18 µA
Distance from chip top to tracking surface	5 ~ 60 mm on glossy metal surfaces 20 ~ 40mm on white copy paper
Light Source	VCSEL LASER 850 nm
Package Size L x W x H	4.4 x 4.6 x 1.0 mm

Ordering Information

Part Number	Package Type
PAT9130EW-TKMT	LGA 10-pin

RoHS compliant

LASER 1

For any additional inquiries, please contact us at
http://www.pixart.com/contact.asp

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1.0 Introduction

1.1 Overview

PAT9130EW-TKMT is a high performance CMOS-processed optical image chip with integrated digital image process circuits. It is based on PixArt LASER-based optical navigation technology which measures changes in position by optically acquiring sequential surface images (frames) and mathematically determining the speed, the direction and the magnitude of motion. The displacement X and Y information are available in registers. A host controller can read and translate the displacement X and Y information from the SPI serial interface.

Note: Throughout this document PAT9130EW-TKMT is referred to as the chip.

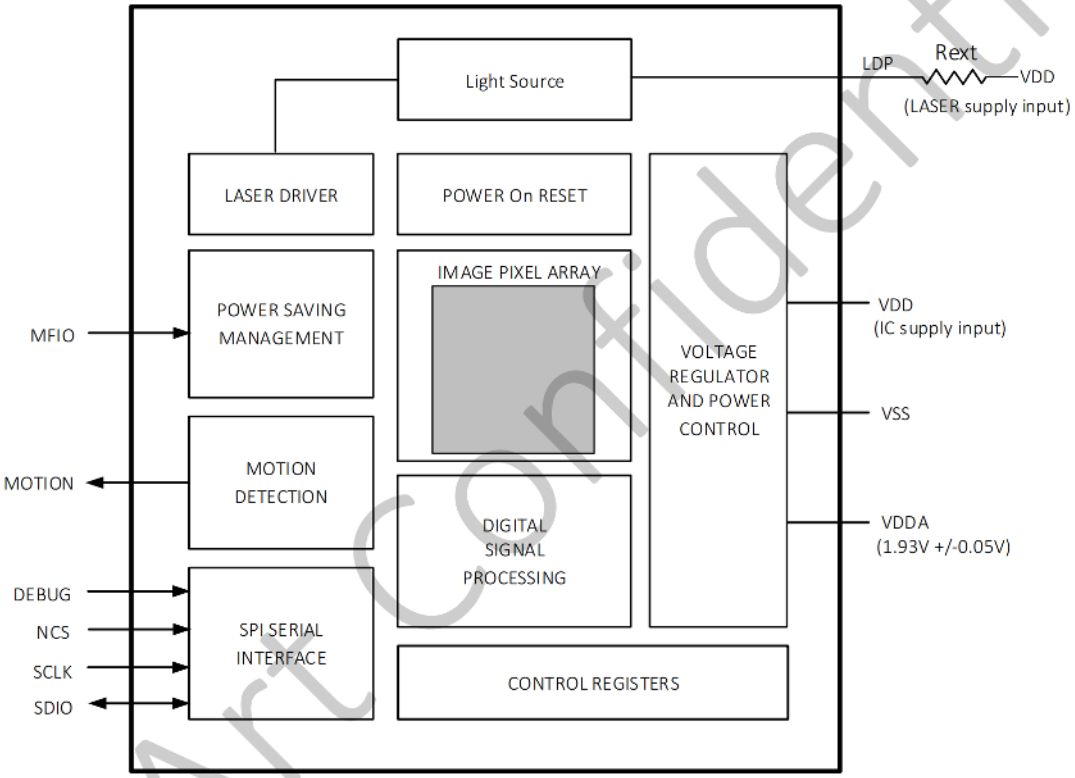
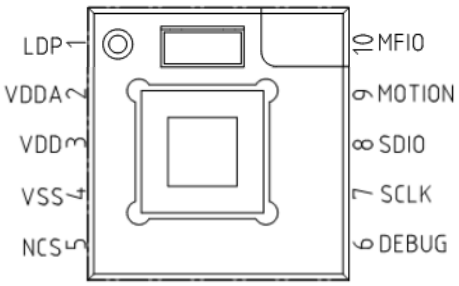


Figure 1. Chip Architecture Functional Block Diagram

1.2 Signal Description



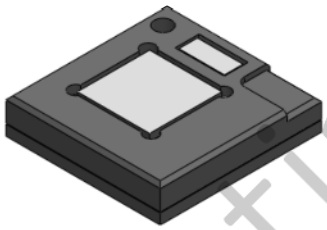


Figure 2. Pinout Configuration

Table 1. Signal Pins Description

Pin No.	Signal Name	Type	Description
1	LDP	PWR	Anode of the VCSEL LASER. This pin should be connected to VDD power supply (2.7V - 3.6V) through a resistor (Rext)
2	VDDA	PWR	Power supply for core circuitry, voltage range : 1.93V +/- 0.05V
3	VDD	PWR	Power supply for I/O and LASER, voltage range : 2.7V ~ 3.6V
4	VSS	GND	Chip ground
5	NCS	IN	Chip select for 3-wire SPI interface (active low)
6	DEBUG	IN	This pin is for debug purpose and is only for PixArt internal use. In normal operation, this pin should connect a 100k ohm resistor to GND.
7	SCLK	IN	Clock input for SPI interface
8	SDIO	I/O	Bi-directional I/O for SPI interface
9	MOTION	OUT	Interrupt output for motion detection (active low)
10	MFIO	IN	Multi-function input pin. This pin can be configured as Power-Down, Reset or Quick-Burst function. Default is Null function. Please tie to GND if this pin is not used (Null function).

2.0 Mechanical Specifications

2.1 Mechanical Dimension

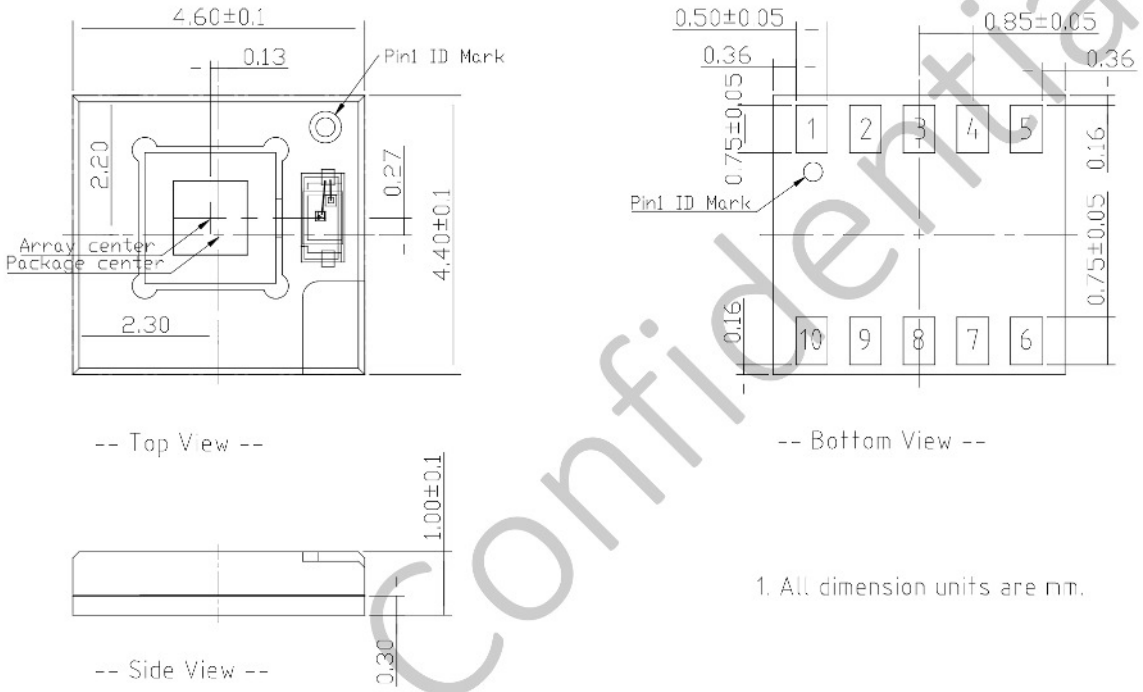


Figure 3. Chip Package Outline Diagram

3.0 Operating Specifications

3.1 Absolute Maximum Ratings

Table 2. Absolute Maximum Ratings

Parameters	Symbol	Min.	Max.	Unit	Notes
Supply Voltage	VDD	-0.3	3.9	V	I/O and LASER power
	VDDA	-0.2	2.3	V	Core circuitry power
ESD	ESD_{HBM}		2	kV	Class 2 on all pins, as per human body model. JESD22-A114E with 15 sec zap interval.

Notes:
1. At room temperature.
2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum-rated conditions is not implied.

3.2 Recommended Operating Conditions

Table 3. Recommended Operating Conditions

Description	Symbol	Min.	Typ.	Max.	Unit	Notes
Storage Temperature	T_{STG}	-40	-	85	°C	
Operating Temperature	T_A	-20	25	60	°C	
Power Supply Voltage	VDD	2.7	3.3	3.6	V	I/O and LASER power supply
	VDDA	1.88V	1.93V	1.98V	V	Core circuitry power supply
Supply Noise (peak to peak)	V_{pp}	-	-	100	mV	Peak to peak voltage within 100KHz – 80MHz
SPI Clock Frequency	SCLK	-	-	2	MHz	
Tracking Speed	SP	-	-	90	IPS	on glossy metal surfaces
				35		on white copy paper
Laser Drive Current (DC)	I_{LD}	5.0	7.0	8.0	mA	Configured via LD_SRC register

Note: PixArt does not guarantee the performance if the operating temperature is beyond the specified limit.

3.3 DC Characteristics

Table 4. DC Electrical Specifications

Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
Power Consumption	I_{VDDRN}	-	0.5	-	mA	VDD current @ run mode
	I_{VDDARN}	-	15	-	mA	VDDA current @run mode
	I_{VDDPD}	-	2	-	µA	VDD current @power down
	I_{VDDAPD}	-	18	-	µA	VDDA current @power down
I/O Input High Voltage	V_{IH}	0.7* V_{DD}	-	-	V	
I/O Input Low Voltage	V_{IL}	-	-	0.3* V_{DD}	V	
I/O Output High Voltage	V_{OH}	V_{DD} -0.4	-	-	V	@I_{OH} = 2mA
I/O Output Low Voltage	V_{OL}	-	-	0.4	V	@I_{OL} = 2mA

Notes: All the parameters are tested under operating conditions: V_{DD} = 3.3V (including LASER current), T_A = 25°C

4.0 Power-up Sequence Requirements

If the VDD and VDDA for the chip are not sourced from the same power supplies input, a power-up sequence is applicable on these two power inputs to avoid excessive current leakage or occurrence of unexpected system instability happening on the chip.

1. VDD must be powered up first or at the same time with VDDA. VDDA can never be powered up earlier than VDD.
2. VDD must be powered down first or at the same time with VDDA. VDDA can never be powered down earlier than VDD.
3. VDDA must always be applied with power supply when VDD is powered.
4. It is recommended to activate the SPI control 10ms after a stable VDDA power supply is applied to the chip.

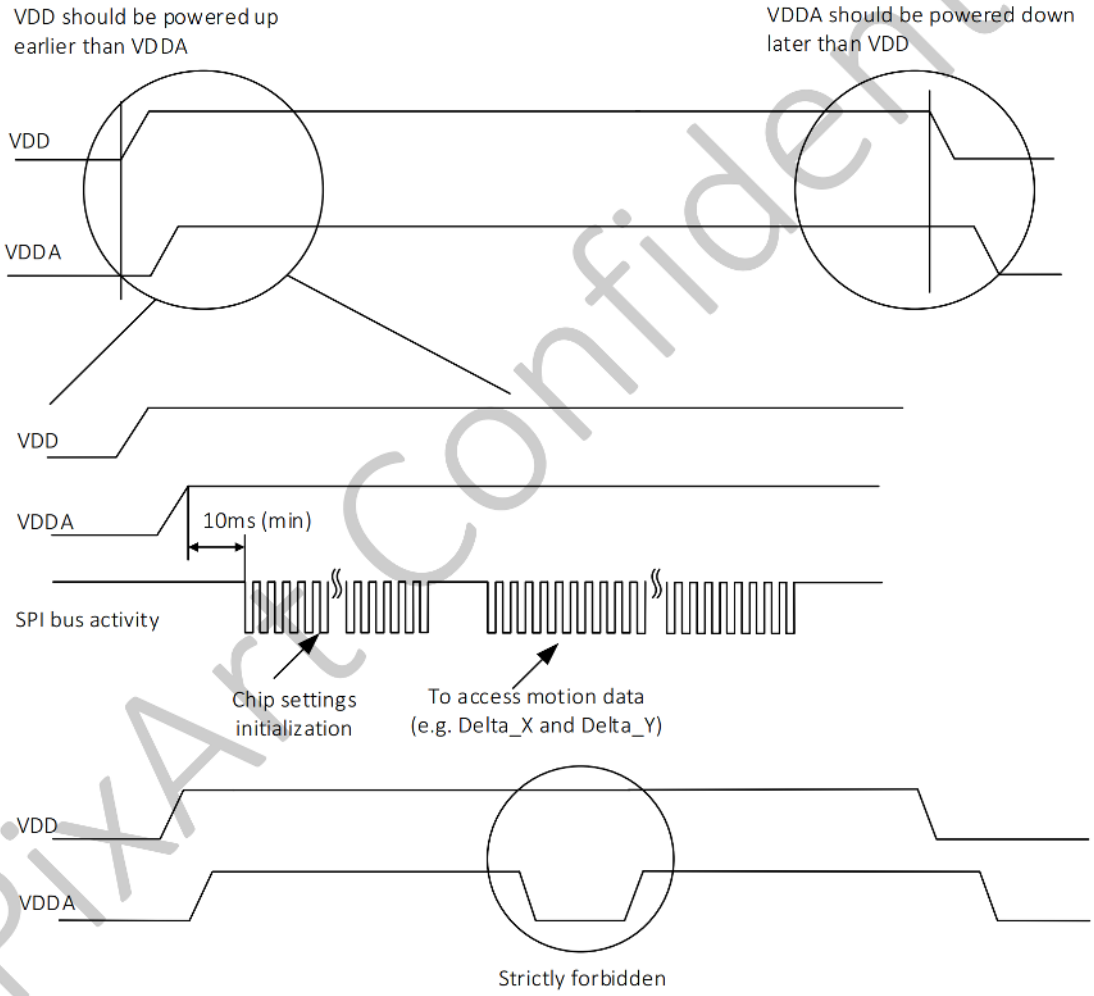
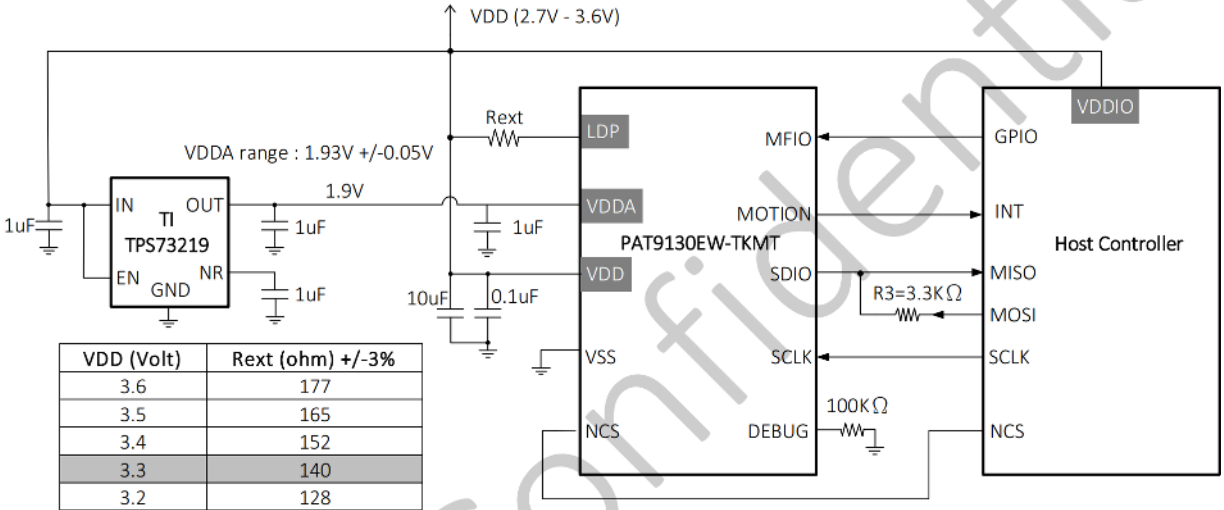


Figure 4. Power-up Sequence Requirements

5.0 Design Reference

5.1 Reference Application Schematics

The chip only supports simplified 3-wire SPI slave mode, while some host controllers may only support standard 4-wire SPI master mode. In this case, users can connect the host controller to the chip using the method shown below to communicate with each other. Take note that the 3.3K ohm resistor is for reference only and the resistance may have to be modified according to different I/O capability as per the specification of the host controllers. The resistor Rext is mandatory to keep the current flowing through the LASER less than 8mA (the LASER max. rating) during the system power-up stage and at any operation condition. Please choose a correct resistance for Rext to match the VDD voltage according to the table below.



VDD (Volt)	Rext (ohm) +/-3%
3.6	177
3.5	165
3.4	152
3.3	140
3.2	128
3.1	115
3.0	102
2.9	90
2.8	78
2.7	65

Figure 5. Reference Application Schematics