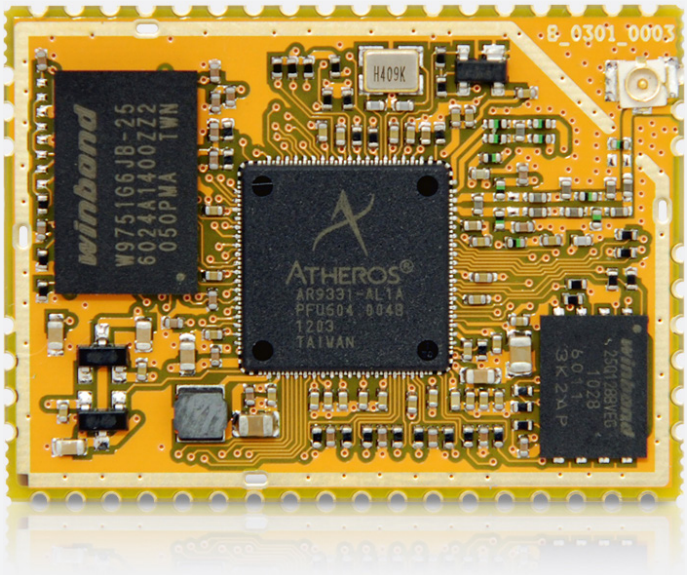
Carambola2 (-I) | Data sheet



Carambola2 is a tiny surface mountable 2.4 GHz Wi-Fi module running OpenWRT linux software

8devices Carambola2 is a member of Carambola wireless modules family and is based on Qualcomm/Atheros AR9331 SoC.

Carambola2 is a surface mountable, single sided, Wi-Fi enabled Linux module, featuring the lowest power consumption in the industry.

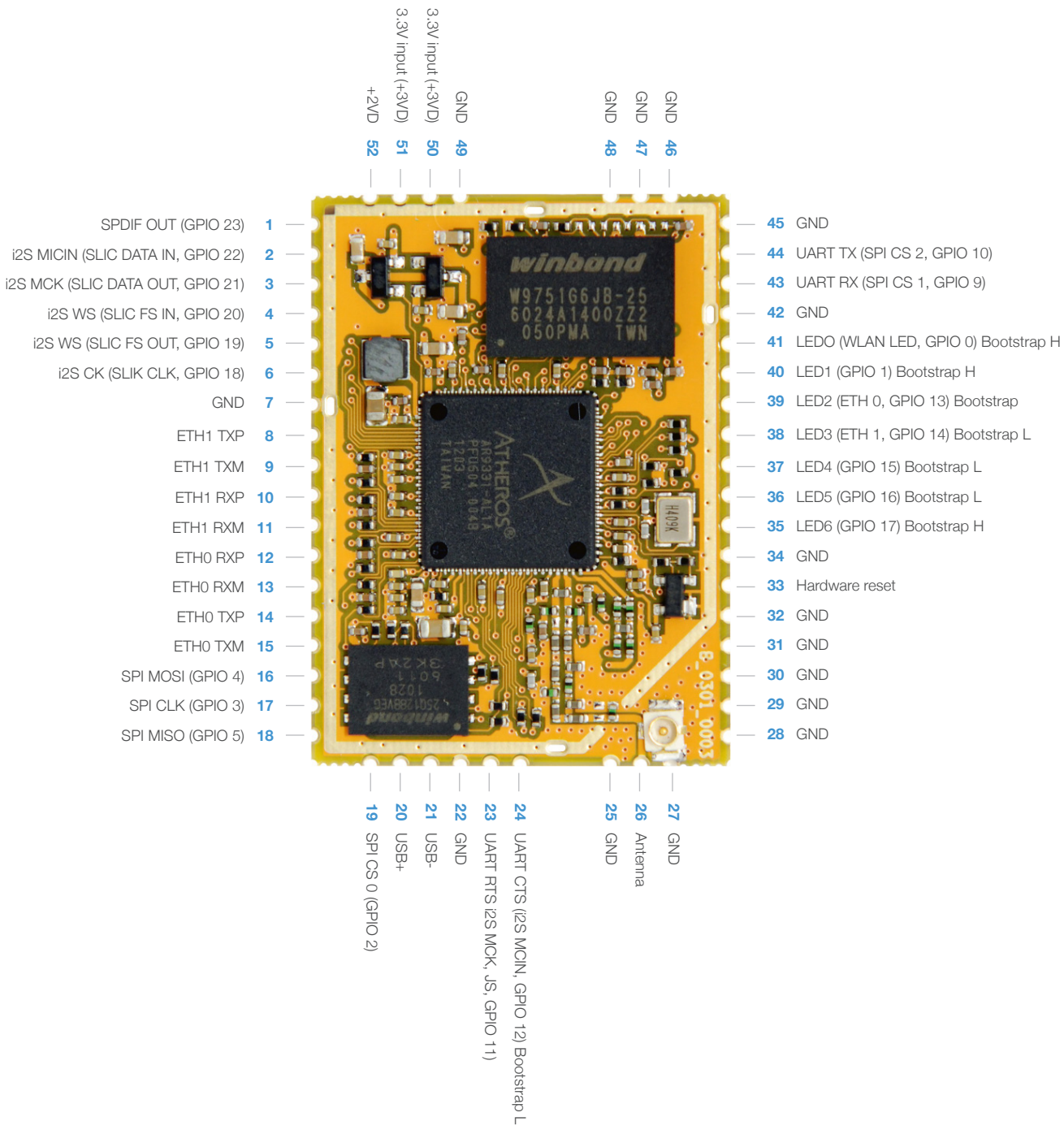
Module comes in two versions:
- Commercial, operating in 0-65 °C (Carambola2)
- Industrial, operating in -40-85 °C (Carambola2-I)

8devices is providing OpenWRT linux distribution source code with necessary patches on GitHub https://github.com/8devices and is supported by our growing community on http://www.8devices.com/community forum.

Quick specs

- 802.11 b/g/n, 2.4 GHz, 1x1 SISO, 150MBps max data rate, 21 dB output power
- U.FL connector or external pin for external antenna
- 16 MB FLASH, 64 MB DDR2 RAM
- Linux friendly , OpenWRT flash image and source code are available for download on www.8devices.com/wiki_carambola
- CPU – AR9331, 400 MHz clock speed
- 28 by 38 mm Size – small and easy to embed
- Surface mountable
- Power supply - 3.3 V, power consumption 0.5 W
- Available interfaces - USB host/slave, serial port,

Pinout Information



Pin	Name	I/O	Description
1	SPDIF OUT (GPIO 23)	O (I/O)	Speaker output
2	i2S MICIN (SLIC DATA IN, GPIO 22)	I (I/O)	Data input (Data transmitted from SLIC to Carambola2)
3	i2S MCK (SLIC DATA OUT, GPIO 21)	O (I/O)	Master clock (Data transmitted from Carambola2 to SLIC)
4	i2S SD (SLIC FS IN, GPIO 20)	I (I/O)	Serial data input/ output (Frame sync in)
5	i2S WS (SLIC FS OUT, GPIO 19)	O (I/O)	Word select for stereo (Frame sync out)
6	i2S CK (SLIC CLK, GPIO 18)	O (I/O)	Stereo clock (SLIC clock)
7	GND	-	Ground connection
8	ETH1 TXP	OA	LAN port 1, positive TX connection
9	ETH1 TXM	OA	LAN port 1, negative TX connection
10	ETH1 RXP	IA	LAN port 1, positive RX connection
11	ETH1 RXM	IA	LAN port 1, negative RX connection
12	ETH0 RXP	IA	LAN port 0, positive RX connection
13	ETH0 RXM	IA	LAN port 0, negative RX connection
14	ETH0 TXP	OA	LAN port 0, positive TX connection
15	ETH0 TXM	OA	LAN port 0, negative TX connection
16	SPI MOSI (GPIO 4)	O (I/O)	Data transmission from the Carambola2 to an external device. On reset, SPI_MOSI (GPIO_4) is output and can directly interface with a SPI device such as a serial flash. If a serial flash is not used, these pins may be used as GPIO pins.
17	SPI CLK (GPIO 3)	O (I/O)	SPI serial interface clock
18	SPI MISO (GPIO 5)	I/O	Data transmission from an external device to the Carambola2. On reset, SPI_MISO (GPIO_5) is input, which should be interfaced with an SPI device via a resistor divider for reliability. If a serial flash is not used, these pins may be used as GPIO pins.
19	SPI CS0 (GPIO 2)	O (I/O)	SPI chip select
20	USB+	IA/OA	Positive USB connection
21	USB-	IA/OA	Negative USB connection
22	GND	-	Ground connection
23	UART RTS (i2S MCK, JS, GPIO 11)	O	UART ready to send signal (Master clock, disables Jumpstart and WPS input function on GPIO11)
24	UART CTS (i2S MCIN, GPIO 12) Bootstrap L	I	UART clear to send signal (Data input)
25	GND	-	Ground connection
26	Antenna	I/O	External antenna connection
27	GND	-	Ground connection
28	GND	-	Ground connection
29	GND	-	Ground connection
30	GND	-	Ground connection
31	GND	-	Ground connection
32	GND	-	Ground connection
33	Hardware reset	I	Hardware reset
34	GND	-	Ground connection
35	LED6 (GPIO 17) Bootstrap H	O (I/O)	Ethernet switch LED5, Bootstrap pin high
36	LED5 (GPIO 16) Bootstrap L	O (I/O)	Ethernet switch LED4, Bootstrap pin low
37	LED4 (GPIO 15) Bootstrap L	O (I/O)	Ethernet switch LED3, Bootstrap pin low
38	LED3 (ETH 1, GPIO 14) Bootstrap L	O (I/O)	Ethernet switch LED2, Bootstrap pin low
39	LED2 (ETH 0, GPIO 13) Bootstrap H	O (I/O)	Ethernet switch LED1, Bootstrap pin high

Pin	Name	I/O	Description
40	LED1 (GPIO 1) Bootstrap H	O (I/O)	WLAN LED2, Bootstrap pin high
41	LED 0 (WLAN LED, GPIO 0) Bootstrap H	O (I/O)	WLAN LED1, Bootstrap pin high
42	GND	-	Ground connection
43	UART RX (SPI CS 1, GPIO 9)	I (O, I/O)	Serial data in (SPI chip select)
44	UART TX (SPI CS 2, GPIO 10)	O (O, I/O)	Serial data out (SPI chip select)
45	GND	-	Ground connection
46	GND	-	Ground connection
47	GND	-	Ground connection
48	GND	-	Ground connection
49	GND	-	Ground connection
50	3.3V input (+3VD)	PI	Input +3.3V
51	3.3V input (+3VD)	PI	Input +3.3V
52	+2VD	PO	+2V Ethernet power supply

IA analog input signal
I digital input signal
I/O digital bidirectional signal
OA analog output signal
O digital output signal
PO power output
PI power input

General GPIO characteristics

Parameter	Units	Min	Max
Output high voltage	V	2.44	2.8
Output low voltage	V	-0	0.1
Input high voltage	V	1.93	3.0
Input low voltage	V	-0.3	0.75

Current drive up to 24 mA.

Bootstrap

Bootstrap HIGH or LOW means that during bootstrap process (first few seconds when the device is turned on) these pins need to be in the specified state. If pins are not in required state then device will not boot correctly.

GPIO

LED GPIO LED0 (GPIO0), LED2 (GPIO13) and LED3 (GPIO14) are being used by kernel module “leds_gpio” - You can use them after removing leds_gpio module by rmmod, or removing it permanently from /etc/modules.d

Free GPIO pins: If you have some hoby project, it is advised to use GPIO pins 18, 19, 20, 21, 22 and 23 without any worries. These pins are not used during the booting process. Other GPIO pins should not be used if you don’t know exactly what you want to achieve, because they are used during the boot process (bootstrap).

SPI interface

SPI interface must be used carefully, it's connected to the internal FLASH memory and CS1 or CS2 must be used.

Power supply

It is recommended to pin 50 and pin 51 for feeding the supply voltage. Use 100nF ceramic capacitors for decoupling.

Software

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Power ratings

For the optimal performance and stability recommended power ratings must be used. Device might malfunction outside minimum and maximum power ratings.

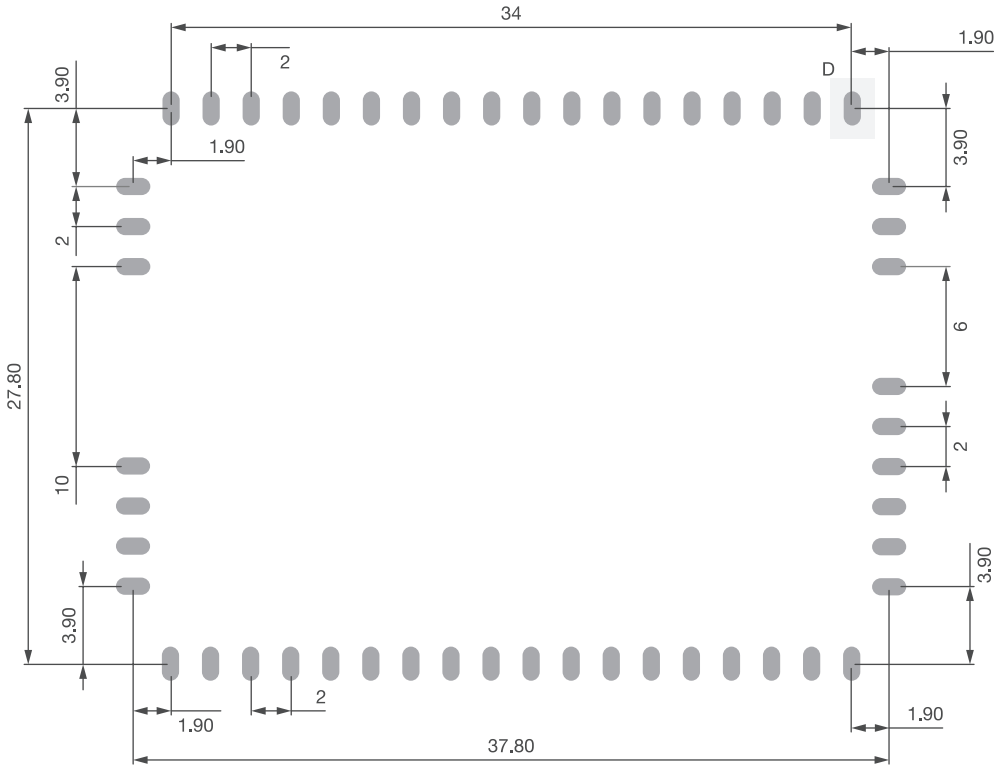
Parameter	Units	Min	Nominal	Max
DC supply voltage	V	2.97	3.3	3.63
Current	A	0.09	0.110	0.450
Network transformer voltage	V	1.9	2.0	2.15

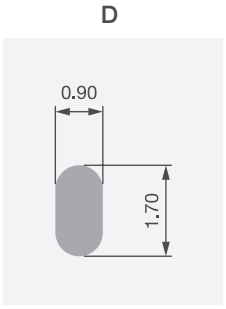
Operating conditions

The module can operate in a wide temperature range and different conditions depending on the enclosure. The following guidelines guarantee that it will work correctly.

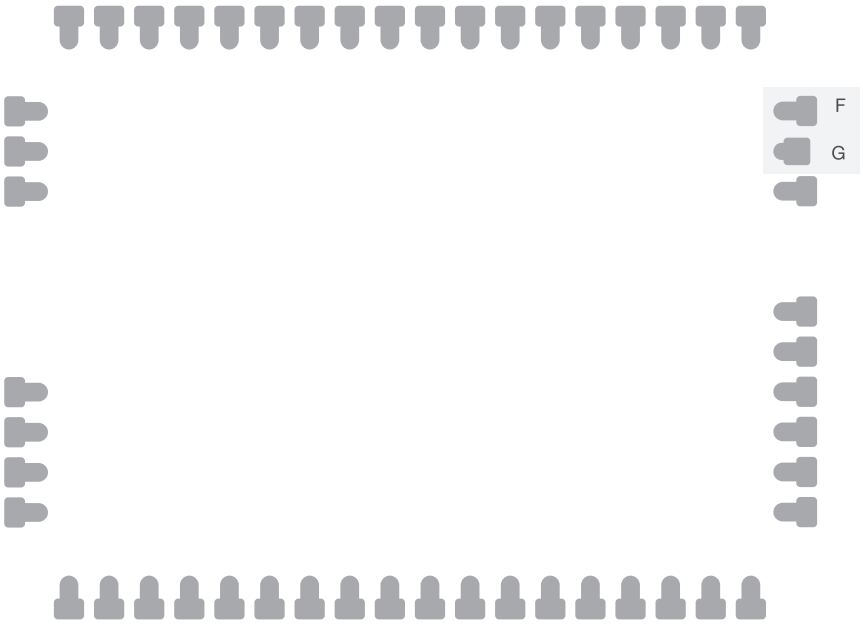
Parameter	Units	Min	Max
Working temperature (Carambola2/Carambola2-I)	C	0/ -40	65/ 85
Storage temperature (Carambola2/Carambola2-I	C	-40	70/ 90
Humidity	%RH	10	90
Storage humidity	%RH	5	90

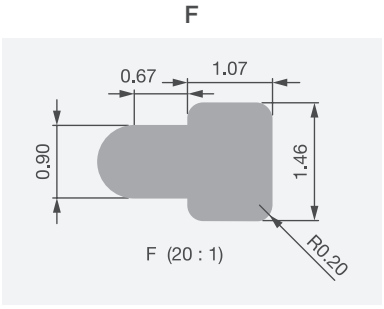
PCB footprint

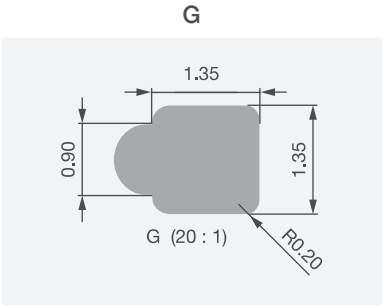




Soldering paste footprint



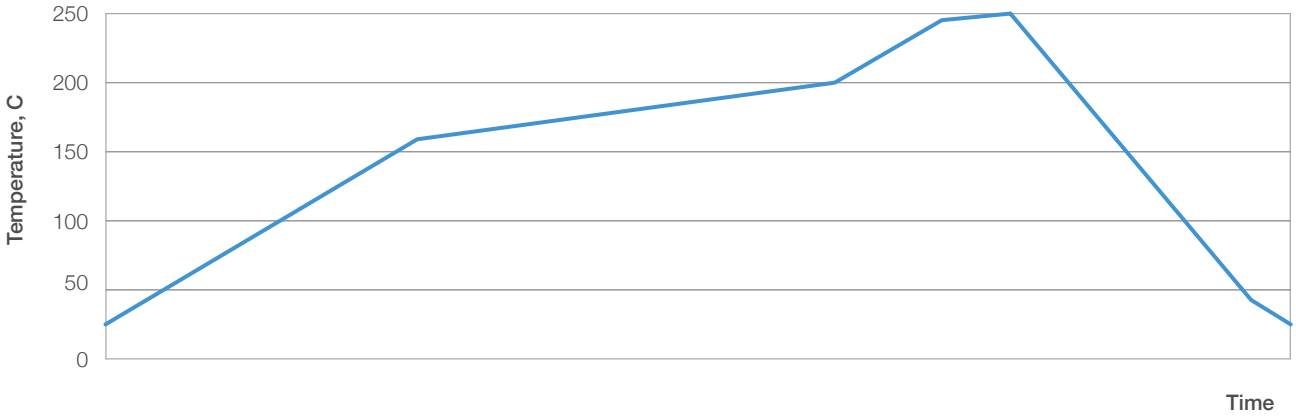




Reflow profile recommendation

Ramp up rate	3°C/second max
Maximum time maintained above 217°C	120 seconds
Peak temperature	250°C
Maximum time within 5°C of peak temperature	20 seconds
Ramp down rate	6°C/second max

Reflow profile

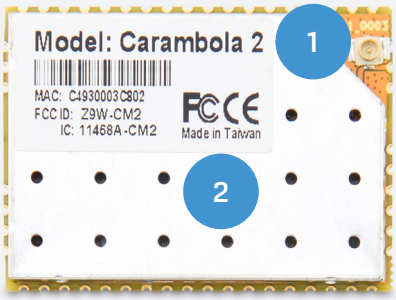


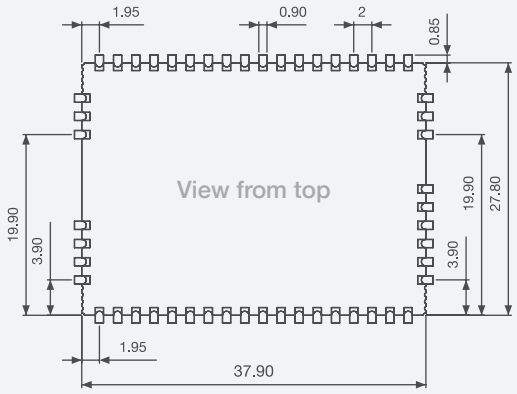
Radio characteristics

Receive sensitivity (dBm)	802.11N (20 MHz)	7.2 Mbps	14.4 Mbps	21.7 Mbps	28.9 Mbps	43.3 Mbps	57.8 Mbps	65 Mbps	72.2 Mbps
		-94	-91	-88	-85	-82	-79	-76	-73
	802.11N (40 MHz)	15 Mbps	30 Mbps	45 Mbps	60 Mbps	90 Mbps	120 Mbps	135 Mbps	150 Mbps
		-89	-86	-83	-80	-78	-75	-72	-69

Output power (dBm)	802.11N 20 MHz	7.2 Mbps	14.4 Mbps	21.7 Mbps	28.9 Mbps	43.3 Mbps	57.8 Mbps	65 Mbps	72.2 Mbps
		21	20	20	19	18	17	16	15
	802.11N 40 MHz	15 Mbps	30 Mbps	45 Mbps	60 Mbps	90 Mbps	120 Mbps	135 Mbps	150 Mbps
		20	19	19	19	18	17	16	15

Carambola2 details

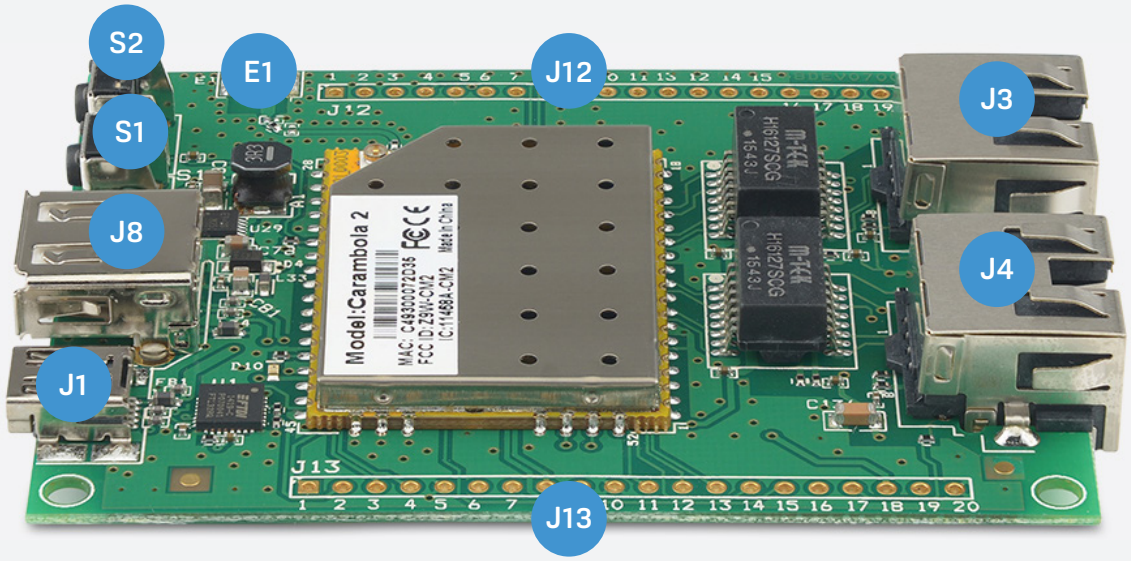




1 Male UFL connector for external antenna

2 RF shield

Carambola2 DVK



E1	Integrated 2.4 GHz chip antenna	**J8**	Type A USB socket
J12, J13	2 x 10 2.54 mm pitch prototyping area holes	**J1**	Mini - A USB socket (console + power 5V)
J3	ETH0 LAN port	**S1**	GPIO programable button
J4	ETH1 LAN port	**S2**	Hardware reset button